

600V High Voltage 3-phase Motor Driver ICs SCM1270MF Series

Data Sheet

Description

The SCM1270MF series are high voltage 3-phase motor driver ICs in which transistors, pre-driver ICs (MICs), and bootstrap circuits (diodes and resistors) are highly integrated.

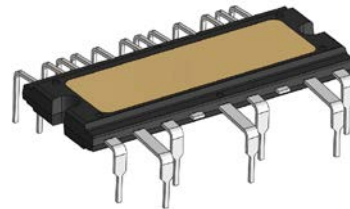
These products can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

- Temperature Sensing Function
- In Case of Abnormal Operation, All Outputs Shut Down via the FO1, FO3, and SD Pins Connected Together
- Built-in Bootstrap Diodes with Current Limiting Resistors (22 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Bare Lead Frame: Pb-free (RoHS compliant)
- Isolation Voltage: 2500 V (for 1 min)
UL-recognized Component (File No.: E118037)
- Fault Signal Output at Protection Activation
- Protections:
 - Undervoltage Lockout for Power Supply
 - High-side (UVLO_VB): Auto-restart
 - Low-side (UVLO_VCC): Auto-restart
 - Overcurrent Protection (OCP): Auto-restart
 - Simultaneous On-state Prevention: Auto-restart

Package

DIP33
Pin Pitch: 1.27 mm
Mold Dimensions: 47 mm × 19 mm × 4.4 mm



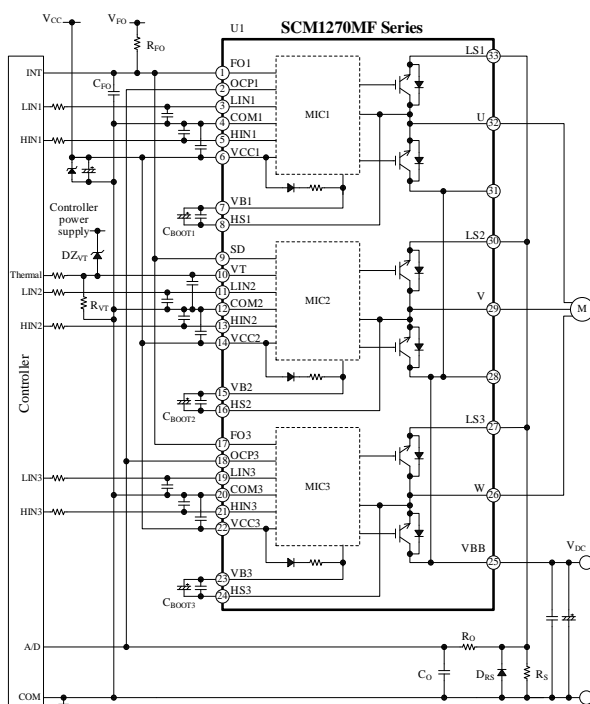
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Selection Guide

- Power Device: IGBT + FRD (600 V)

Output DC Current	Part Number
10 A	SCM1271MF
15 A	SCM1272MF
20 A	SCM1274MF
30 A	SCM1276MF

Typical Application



Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Air Conditioner Compressor Motor
- Washing Machine Main Motor
- Fan Motor
- Pump Motor

Contents

Description	1
Contents	2
1. Absolute Maximum Ratings	4
2. Recommended Operating Conditions	5
3. Electrical Characteristics	6
3.1. Characteristics of Control Parts	6
3.2. Bootstrap Diode Characteristics	7
3.3. Thermal Resistance Characteristics	7
3.4. Transistor Characteristics	8
3.4.1. SCM1271MF	8
3.4.2. SCM1272MF	9
3.4.3. SCM1274MF	9
3.4.4. SCM1276MF	10
4. Mechanical Characteristics	11
5. Insulation Distance	11
6. Truth Table	12
7. Block Diagram	13
8. Pin Configuration Definitions	14
9. Typical Application	15
10. Physical Dimensions	17
10.1. LF2552	17
10.2. Leadform 2557 (Long Lead Type)	18
10.3. Reference PCB Hole Sizes	19
11. Marking Diagram	19
12. Functional Descriptions	20
12.1. Turning On and Off the IC	20
12.2. Pin Descriptions	20
12.2.1. U, V, and W	20
12.2.2. VB1, VB2, and VB3	20
12.2.3. HS1, HS2, and HS3	21
12.2.4. VCC1, VCC2, and VCC3	21
12.2.5. COM1, COM2, and COM3	21
12.2.6. HIN1, HIN2, and HIN3 LIN1, LIN2, and LIN3	21
12.2.7. VBB	22
12.2.8. LS1, LS2, and LS3	22
12.2.9. OCP1 and OCP3	23
12.2.10. FO1 (for U-phase) and FO3 (for W-phase)	23
12.2.11. SD (for V-phase)	24
12.2.12. VT24	
12.3. Temperature Sensing Function	24
12.4. Protections	25
12.4.1. Fault Signal Output	25
12.4.2. Shutdown Signal Input	25
12.4.3. Undervoltage Lockout for Power Supply (UVLO)	25
12.4.4. Overcurrent Protection (OCP)	27
12.4.5. Simultaneous On-state Prevention	28
13. Design Notes	29
13.1. PCB Pattern Layout	29

SCM1270MF Series

13.2. Considerations in Heatsink Mounting	29
13.3. Considerations in IC Characteristics Measurement	29
14. Calculating Power Losses and Estimating Junction Temperature	30
14.1. IGBT Steady-state Loss, P_{ON}	30
14.2. IGBT Switching Loss, P_{SW}	31
14.3. Estimating Junction Temperature of IGBT	31
15. Performance Curves	32
15.1. Transient Thermal Resistance Curves	32
15.1.1. SCM1271MF	32
15.1.2. SCM1272MF, SCM1274MF, and SCM1276MF	32
15.2. Performance Curves of Control Parts	33
15.3. Performance Curves of Output Parts	38
15.3.1. Output Transistor Performance Curves	38
15.3.2. Switching Losses	40
15.4. Allowable Effective Current Curves	44
15.4.1. SCM1271MF	44
15.4.2. SCM1272MF	45
15.4.3. SCM1274MF	46
15.4.4. SCM1276MF	47
15.5. Short Circuit SOAs (Safe Operating Areas)	48
15.5.1. SCM1271MF	48
15.5.2. SCM1272MF	48
15.5.3. SCM1274MF	49
15.5.4. SCM1276MF	49
16. Pattern Layout Example	50
17. Typical Motor Driver Application	52
Important Notes	53

SCM1270MF Series

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

Unless specifically noted, $T_A = 25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB-LS1, VBB-LS2, VBB-LS3	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB-LS1, VBB-LS2, VBB-LS3	500	V	
IGBT Breakdown Voltage	V_{CES}	$V_{CC} = 15\text{ V}$, $I_C = 1\text{ mA}$, $V_{IN} = 0\text{ V}$	600	V	
Logic Supply Voltage	V_{CC}	VCC1-COM1, VCC2-COM2, VCC3-COM3	20	V	
	V_{BS}	VB1-HS1(U), VB2-HS2(V), VB3-HS3(W)	20		
Output Current ⁽¹⁾	I_O	$T_C = 25\text{ }^{\circ}\text{C}$	10	A	SCM1271MF
			15		SCM1272MF
			20		SCM1274MF
			30		SCM1276MF
Output Current (Pulse)	I_{OP}	$T_C = 25\text{ }^{\circ}\text{C}$, $P_w \leq 1\text{ ms}$, single pulse	20	A	SCM1271MF
			30		SCM1272MF SCM1274MF
			45		SCM1276MF
Input Voltage	V_{IN}	HIN1/LIN1-COM1, HIN2/LIN2-COM2, HIN3/LIN3-COM3	-0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO1-COM1, FO3-COM3	-0.5 to 7	V	
SD Pin Voltage	V_{SD}	SD-COM2	-0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCP1-COM1, OCP3-COM3	-10 to 5	V	
Operating Case Temperature ⁽²⁾	$T_{C(OP)}$		-30 to 125	$^{\circ}\text{C}$	
Junction Temperature ⁽³⁾	T_j		150	$^{\circ}\text{C}$	
Storage Temperature	T_{stg}		-40 to 150	$^{\circ}\text{C}$	
Isolation Voltage ⁽⁴⁾	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V	

⁽¹⁾ Should be derated depending on an actual case temperature. See Section 15.4.

⁽²⁾ Refers to a case temperature measured during IC operation.

⁽³⁾ Refers to the junction temperature of each chip built in the IC, including the monolithic IC (MIC), transistors, and freewheeling diodes.

⁽⁴⁾ Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

SCM1270MF Series

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	COM1 = COM2 = COM3, VBB-COM	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCC1-COM1, VCC2-COM2, VCC3-COM3	13.5	—	16.5	V	
	V_{BS}	VB1-HS1(U), VB2-HS2(V), VB3-HS3(W)	13.5	—	16.5	V	
Input Voltage (HINx, LINx, FOx, and SD)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	μ s	
	$t_{IN(MIN)OFF}$		0.5	—	—	μ s	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	μ s	
FO Pin Pull-up Resistor	R_{FO}		1	—	22	k Ω	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		—	—	1000	pF	
VT Pin Pull-down Resistor	R_{VT}		10	—	—	k Ω	
Bootstrap Capacitor	C_{BOOT}		10	—	220	μ F	
Shunt Resistor	R_S	$I_p \leq 45$ A	12	—	—	m Ω	SCM1276MF
		$I_p \leq 30$ A	18	—	—		SCM1272MF SCM1274MF
		$I_p \leq 20$ A	27	—	—		SCM1271MF
RC Filter Resistor	R_O	*	—	—	100	Ω	
RC Filter Capacitor	C_O	*	—	—	8200	pF	
PWM Carrier Frequency	f_C		—	—	20	kHz	

* R_O and C_O must be chosen the values that satisfy $R_O \times C_O < 0.82 \mu$ s (see Section 12.4.4).

SCM1270MF Series

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (-).

Unless otherwise specified, $T_A = 25\text{ }^\circ\text{C}$ and $V_{CC} = 15\text{ V}$.

3.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1-COM1, VCC2-COM2, VCC3-COM3	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VB1-HS1(U), VB2-HS2(V), VB3-HS3(W)	10.5	11.5	12.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1-COM1, VCC2-COM2, VCC3-COM3	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VB1-HS1(U), VB2-HS2(V), VB3-HS3(W)	10.0	11.0	12.0	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2 = VCC3, COM1 = COM2 = COM3, VCC pin current in 3-phase operation	—	3	—	mA	
	I_{BS}	VB-HS = 15 V, HIN = 5 V, VBx pin current in 1-phase operation	—	140	—	μA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, FOx, and SD)	V_{IH}		1.5	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, FOx, and SD)	V_{IL}		1.0	1.5	2.0	V	
High Level Input Current (HINx and LINx)	I_{IH}	$V_{IN} = 5\text{ V}$	—	230	500	μA	
Low Level Input Current (HINx and LINx)	I_{IL}	$V_{IN} = 0\text{ V}$	—	—	2	μA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	$V_{FO} = 5\text{ V}$, $R_{FO} = 10\text{ k}\Omega$	—	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	$V_{FO} = 5\text{ V}$, $R_{FO} = 10\text{ k}\Omega$	4.8	—	—	V	
Protection							
Overcurrent Protection Threshold Voltage	V_{TRIP}		0.46	0.50	0.54	V	
Overcurrent Protection Hold Time	t_p		20	26	—	μs	
Overcurrent Protection Blanking Time	t_{BK}	$V_{TRIP} = 1\text{ V}$	—	370	—	ns	
SD Pin Filtering Time	$t_{FIL(SD)}$		135	300	—	ns	
Temperature Sensing Voltage*	V_T	$T_{j(MIC)} = 125\text{ }^\circ\text{C}$, $V_{RT} = 10\text{ k}\Omega$	2.69	2.75	2.81	V	

* V_T is determined by the junction temperature of the control parts (not the junction temperature of output transistors).

3.2. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	$V_R = 600 \text{ V}$	—	—	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	$I_{FB} = 0.15 \text{ A}$	—	1.1	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		17.6	22.0	26.4	Ω	

3.3. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance ⁽¹⁾	$R_{(j-c)Q}$ ⁽²⁾	1 element operation (IGBT)	—	—	3.7	$^{\circ}\text{C/W}$	SCM1271MF
			—	—	3		SCM1272MF SCM1274MF SCM1276MF
	$R_{(j-c)F}$ ⁽³⁾	1 element operation (freewheeling diode)	—	—	4.5	$^{\circ}\text{C/W}$	SCM1271MF
			—	—	4		SCM1272MF SCM1274MF SCM1276MF

- ⁽¹⁾ Refers to a case temperature at the measurement point described in Figure 3-1, below.
- ⁽²⁾ Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.
- ⁽³⁾ Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

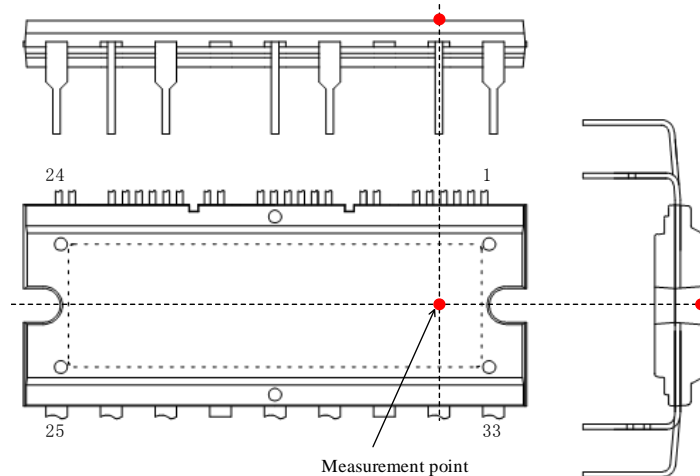


Figure 3-1. Case Temperature Measurement Point

3.4. Transistor Characteristics

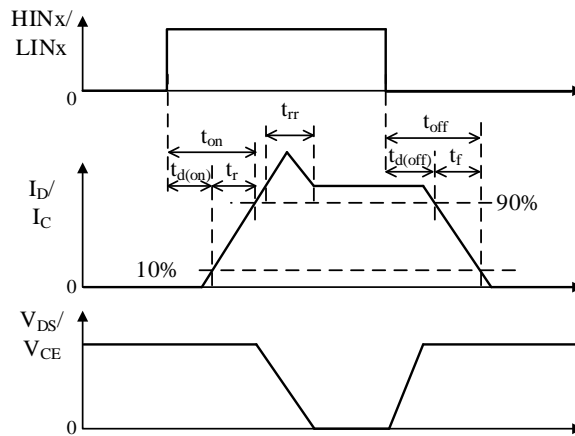


Figure 3-2. Switching Characteristics Definitions

3.4.1. SCM1271MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	$V_{CE} = 600 \text{ V}, V_{IN} = 0 \text{ V}$	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 10 \text{ A}, V_{IN} = 5 \text{ V}$	—	1.7	2.2	V
Diode Forward Voltage	V_F	$I_F = 10 \text{ A}, V_{IN} = 0 \text{ V}$	—	1.7	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 10 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V}$ or $5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1100	—	ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 10 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V}$ or $5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1000	—	ns
Fall Time	t_f		—	100	—	ns

SCM1270MF Series

3.4.2. SCM1272MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	$V_{CE} = 600 \text{ V}, V_{IN} = 0 \text{ V}$	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 15 \text{ A}, V_{IN} = 5 \text{ V}$	—	1.7	2.2	V
Diode Forward Voltage	V_F	$I_F = 15 \text{ A}, V_{IN} = 0 \text{ V}$	—	1.75	2.2	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 15 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200	—	ns
Fall Time	t_f		—	100	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 15 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	800	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200	—	ns
Fall Time	t_f		—	100	—	ns

3.4.3. SCM1274MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	$V_{CE} = 600 \text{ V}, V_{IN} = 0 \text{ V}$	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 20 \text{ A}, V_{IN} = 5 \text{ V}$	—	1.7	2.2	V
Diode Forward Voltage	V_F	$I_F = 20 \text{ A}, V_{IN} = 0 \text{ V}$	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 20 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	900	—	ns
Rise Time	t_r		—	160	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1300	—	ns
Fall Time	t_f		—	120	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 20 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	900	—	ns
Rise Time	t_r		—	190	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1300	—	ns
Fall Time	t_f		—	120	—	ns

SCM1270MF Series

3.4.4. SCM1276MF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	$V_{CE} = 600 \text{ V}, V_{IN} = 0 \text{ V}$	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 30 \text{ A}, V_{IN} = 5 \text{ V}$	—	1.7	2.2	V
Diode Forward Voltage	V_F	$I_F = 30 \text{ A}, V_{IN} = 0 \text{ V}$	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 30 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	800	—	ns
Rise Time	t_r		—	150	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200	—	ns
Fall Time	t_f		—	170	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	$V_{DC} = 300 \text{ V}, I_C = 30 \text{ A},$ $V_{IN} = 0 \rightarrow 5 \text{ V or } 5 \rightarrow 0 \text{ V},$ $T_j = 25 \text{ }^\circ\text{C},$ inductive load	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	800	—	ns
Rise Time	t_r		—	180	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	1200	—	ns
Fall Time	t_f		—	190	—	ns

SCM1270MF Series

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Heatsink Mounting Screw Torque	*	0.588	—	0.784	N·m
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	200	μm
Package Weight		—	11.8	—	g

* When mounting a heatsink, it is recommended to use a metric screw of M3 and a plain washer of 7 mm (φ) together at each end of it. For more details about screw tightening, see Section 13.2.

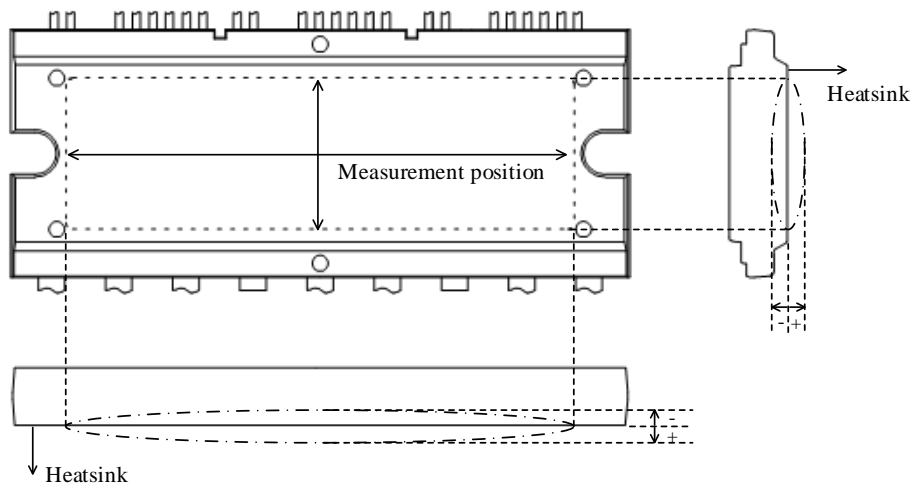


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Clearance	Between heatsink* and leads.	2.0	—	2.5	mm
Creepage	See Figure 5-1.	3.86	—	4.26	mm

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

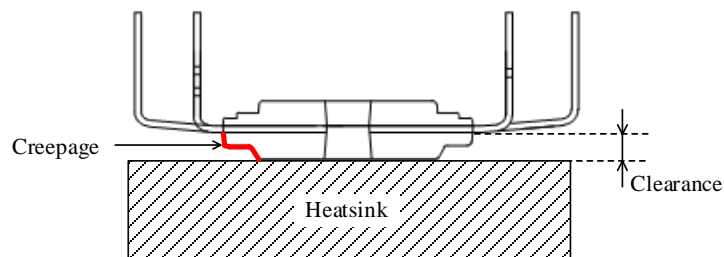


Figure 5-1. Insulation Distance Definitions

6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, the Simultaneous On-state Prevention sets both the high- and low-side transistors off.

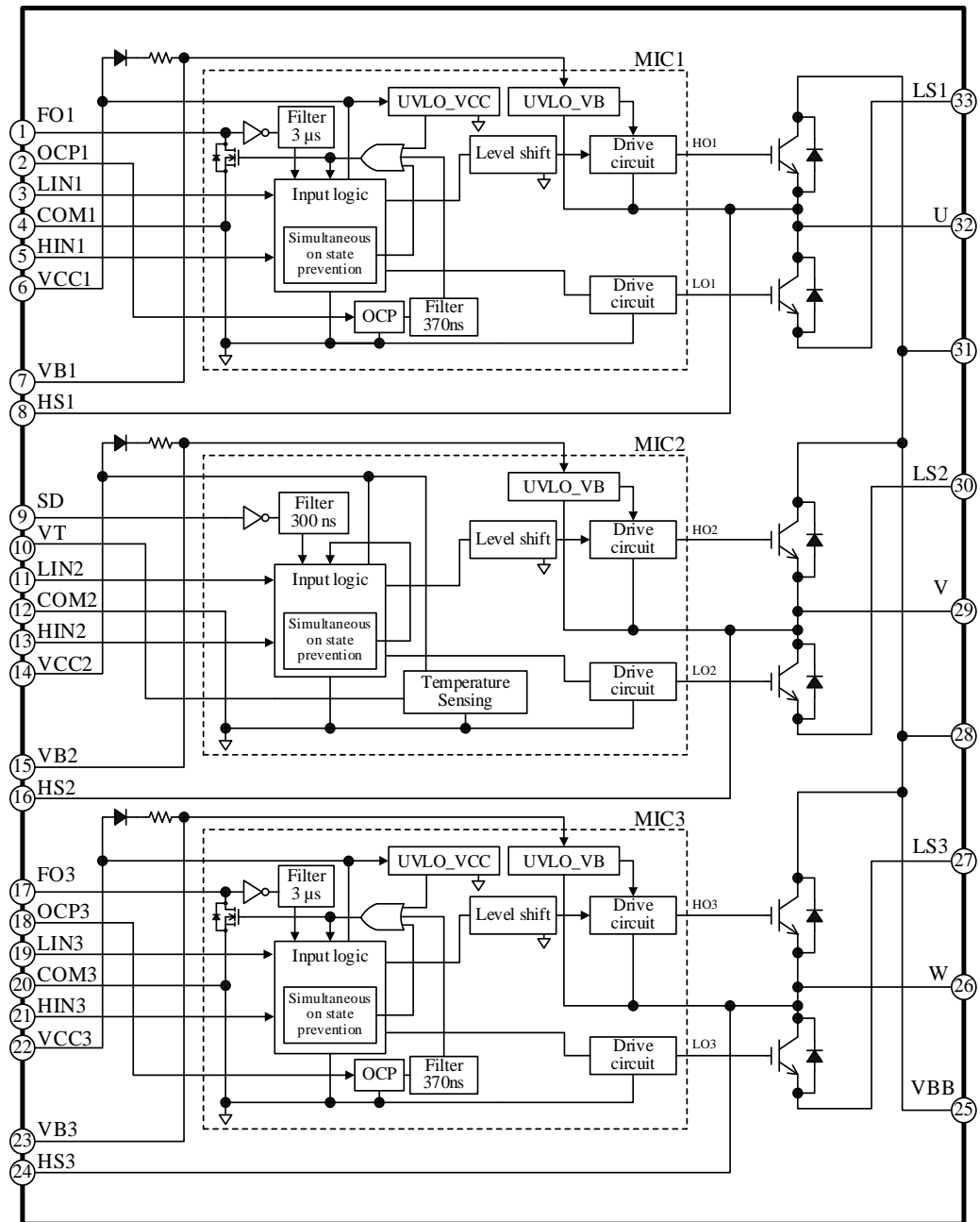
After the IC recovers from a UVLO_VCC condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

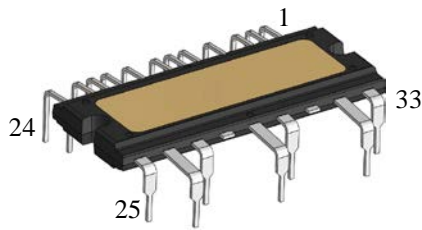
Table 6-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Shutdown Signal Input FO1/FO3/SD = L	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF

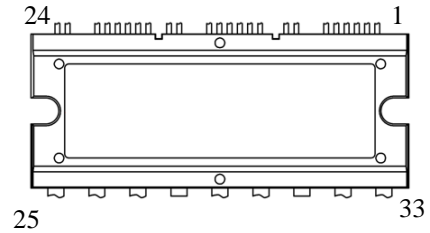
7. Block Diagram



8. Pin Configuration Definitions



Top view



Pin Number	Pin Name	Function
1	FO1	U-phase fault output and shutdown signal input
2	OCP1	Input for U-phase Overcurrent Protection
3	LIN1	Logic input for U-phase low-side gate driver
4	COM1	U-phase logic ground
5	HIN1	Logic input for U-phase high-side gate driver
6	VCC1	U-phase logic supply voltage input
7	VB1	U-phase high-side floating supply voltage input
8	HS1	U-phase high-side floating supply ground
9	SD	V-phase shutdown signal input
10	VT	Temperature sensing voltage output
11	LIN2	Logic input for V-phase low-side gate driver
12	COM2	V-phase logic ground
13	HIN2	Logic input for V-phase high-side gate driver
14	VCC2	V-phase logic supply voltage input
15	VB2	V-phase high-side floating supply voltage input
16	HS2	V-phase high-side floating supply ground
17	FO3	W-phase fault output and shutdown signal input
18	OCP3	Input for W-phase Overcurrent Protection
19	LIN3	Logic input for W-phase low-side gate driver
20	COM3	W-phase logic ground
21	HIN3	Logic input for W-phase high-side gate driver
22	VCC3	W-phase logic supply voltage input
23	VB3	W-phase high-side floating supply voltage input
24	HS3	W-phase high-side floating supply ground
25	VBB	Positive DC bus supply voltage
26	W	W-phase output
27	LS3	W-phase IGBT emitter
28	VBB	(Pin trimmed) positive DC bus supply voltage
29	V	V-phase output
30	LS2	V-phase IGBT emitter
31	VBB	(Pin trimmed) positive DC bus supply voltage
32	U	U-phase output
33	LS1	U-phase IGBT emitter

9. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

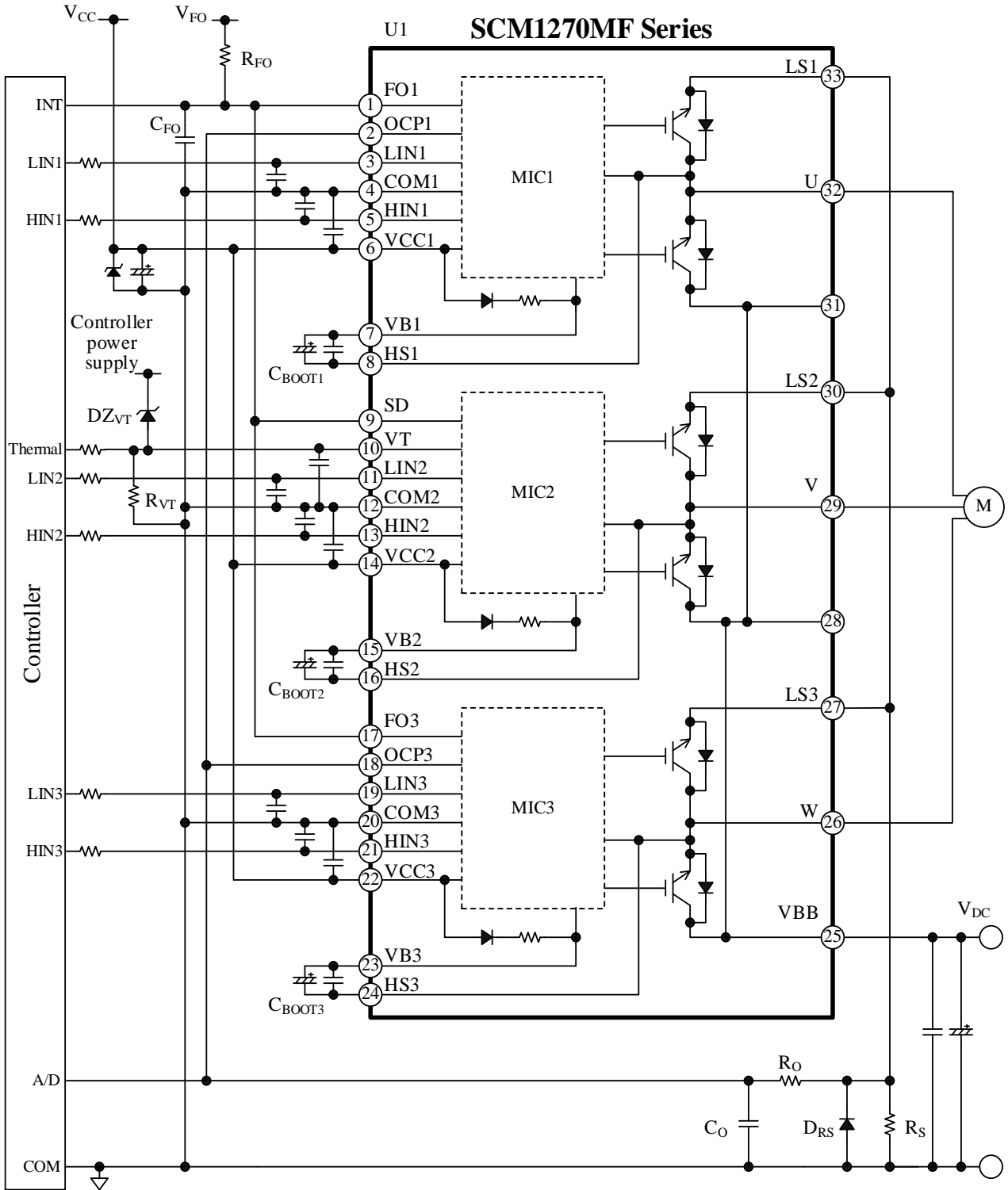


Figure 9-1. Typical Application using a Single Shunt Resistor

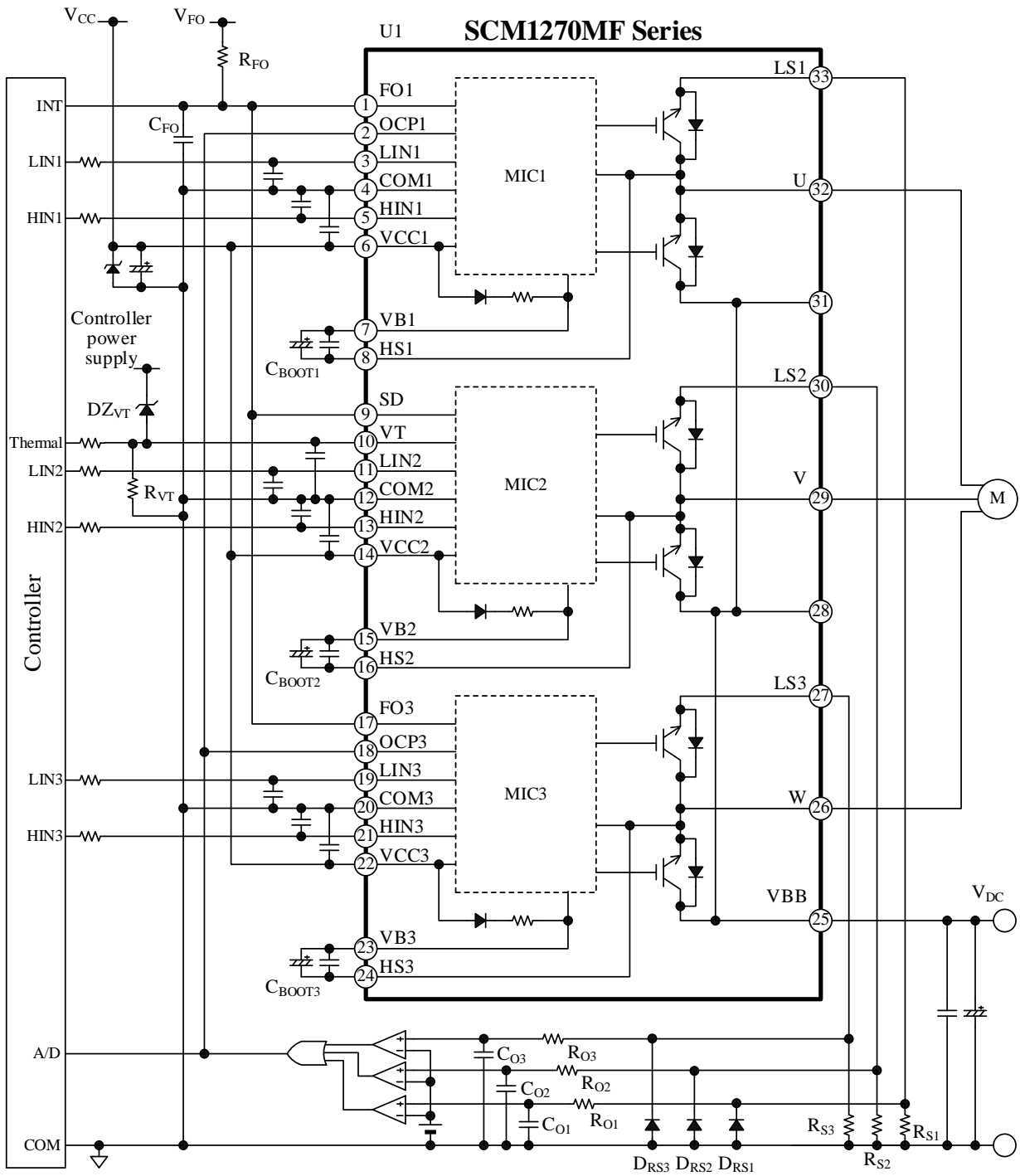
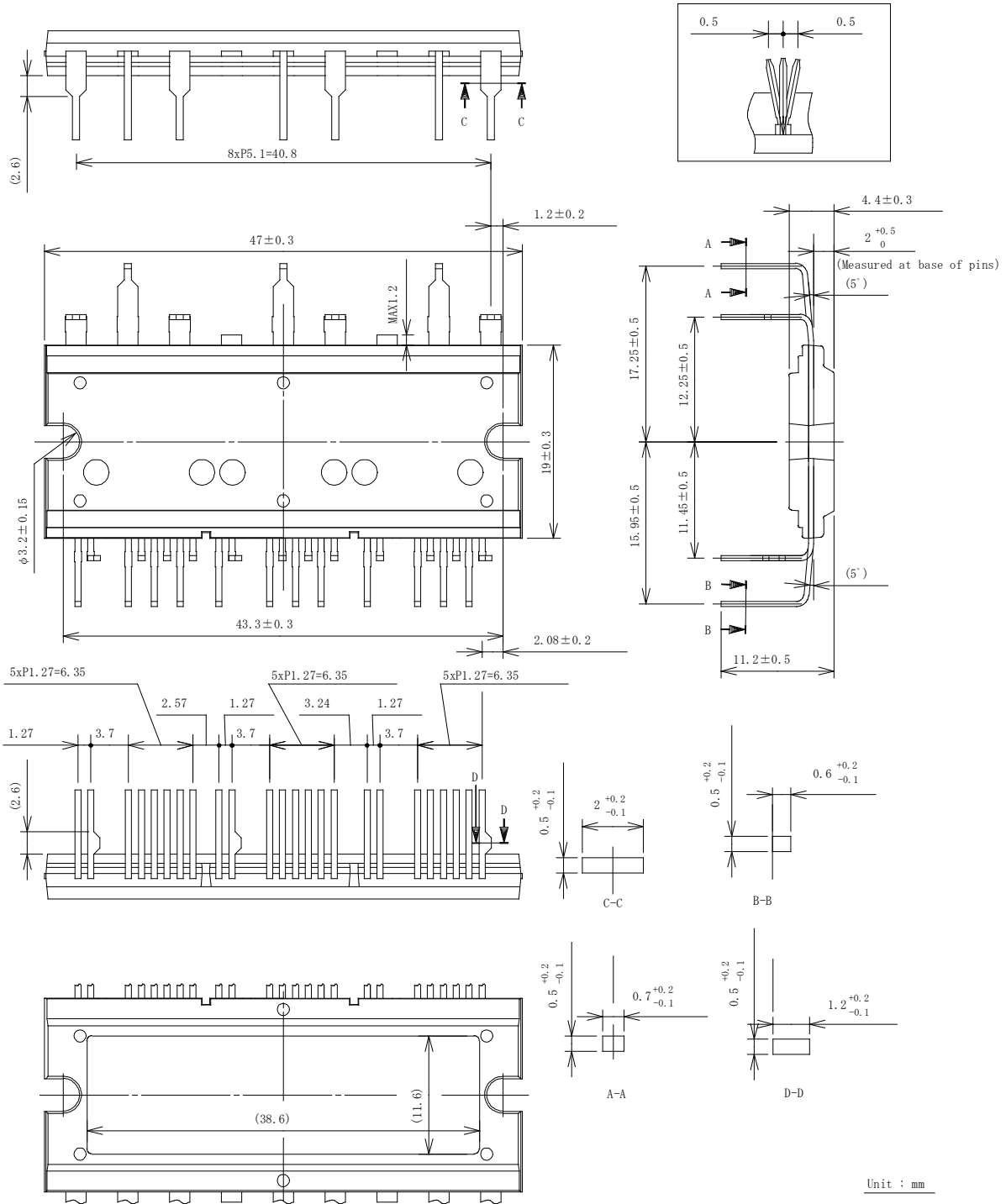


Figure 9-2. Typical Application using Three Shunt Resistors

10. Physical Dimensions

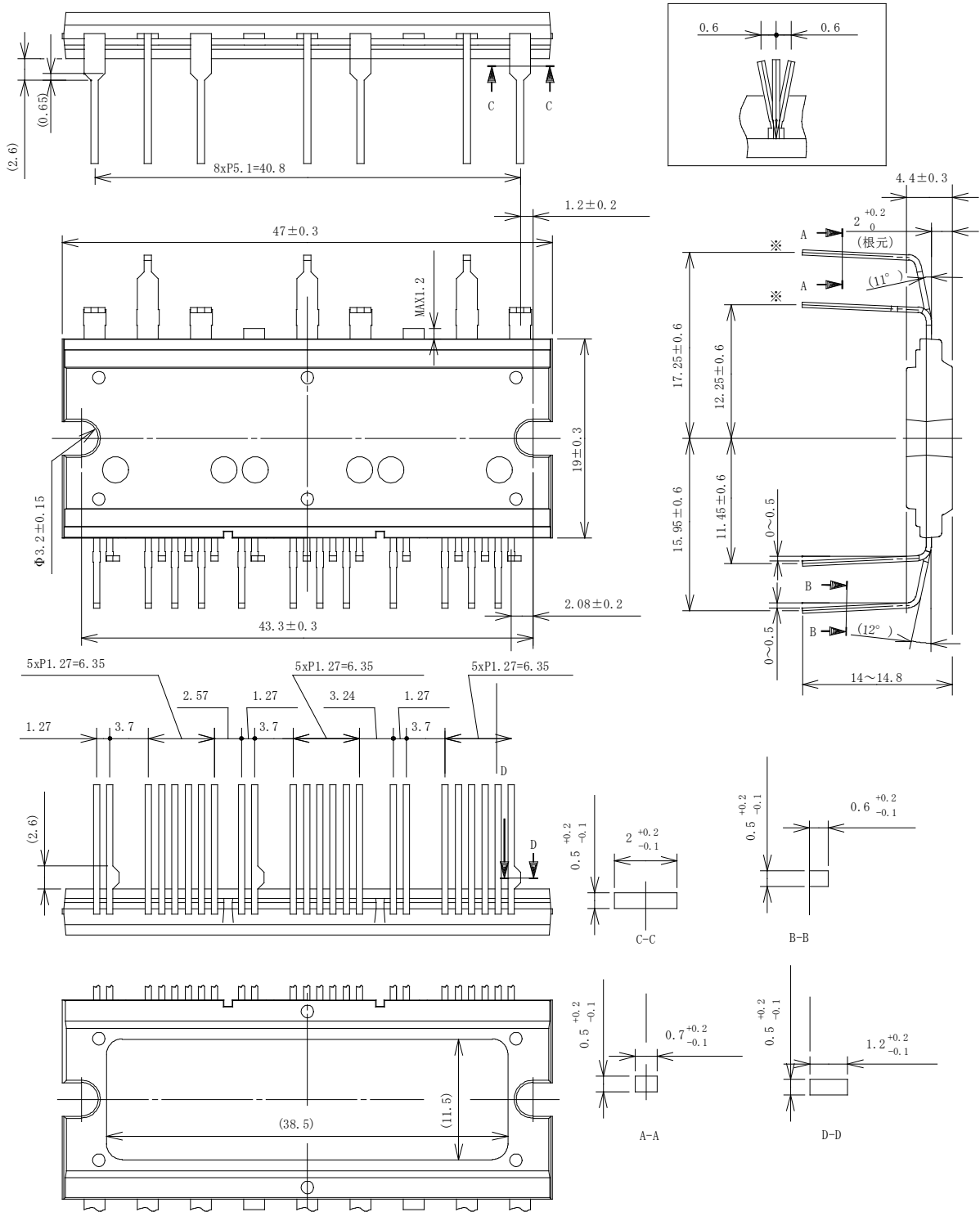
10.1. LF2552



Unit : mm

SCM1270MF Series

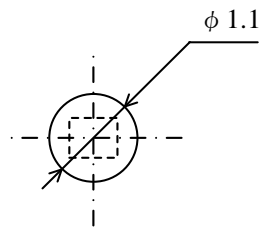
10.2. Leadform 2557 (Long Lead Type)



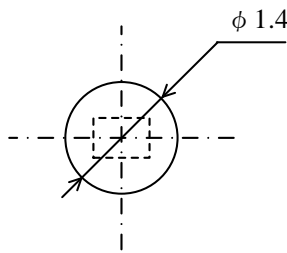
Unit : mm

SCM1270MF Series

10.3. Reference PCB Hole Sizes

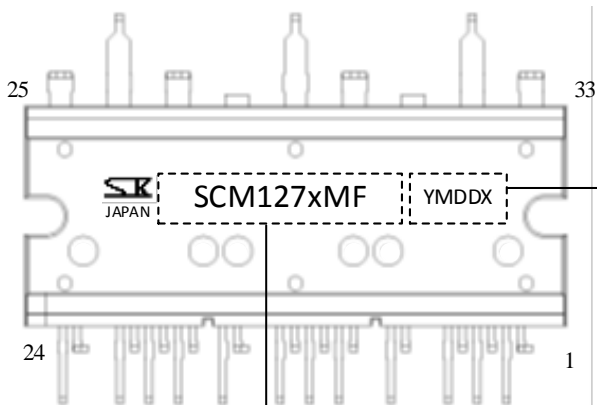
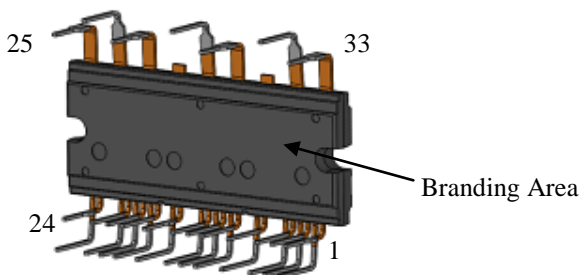


Pins 1 to 24



Pins 25 to 33

11. Marking Diagram



Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

Part Number

12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

For pin descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter “x”, depending on context. The U, V, and W phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, “the VBx pin” is used when referring to either of the VB1, VB2, or VB3 pin. Also, when different pin names are mentioned as a pair (e.g., “the VBx and HSx pins”), they are meant to be the pins in the same phase.

12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to charge bootstrap capacitors, C_{BOOTx} , up to full capacity at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or “L”), and then decrease the VCCx pin voltage.

12.2. Pin Descriptions

12.2.1. U, V, and W

These pins are the outputs of the three phases, and serve as connection terminals to the 3-phase motor. The U, V, and W pins are internally connected to the HS1, HS2, and HS3 pins, respectively.

12.2.2. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases. Voltages across the VBx and HSx pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

In each phase, a bootstrap capacitor, C_{BOOTx} , should be connected between the VBx and HSx pins. For proper startup, turn on the low-side transistor first, then charge the bootstrap capacitor, C_{BOOTx} , up to its maximum capacity. For capacitance of the bootstrap capacitors, C_{BOOTx} , choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose the appropriate values for C_{BOOTx} .

$$C_{BOOT} (\mu F) > 800 \times t_{L(OFF)} (s) \tag{1}$$

$$10 \mu F \leq C_{BOOTx} \leq 220 \mu F \tag{2}$$

In Equation(1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even during the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.4.3.1).

Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 12.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, in each trace between the VCCx and VBx pins, a bootstrap diode, D_{BOOTx} , and a current-limiting resistor, R_{BOOTx} , are placed in series. Time constant for the charging time of C_{BOOTx} , τ , can be computed by Equation (3):

$$\tau = C_{BOOTx} \times R_{BOOTx} \tag{3}$$

where C_{BOOTx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor ($22 \Omega \pm 20\%$).

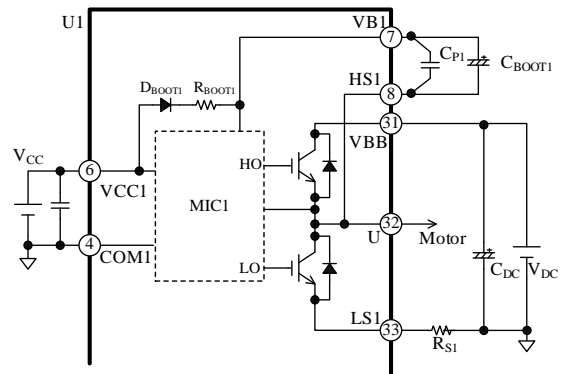


Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit that produces high-side output signals, HOx. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a “Set” signal is generated. When the HINx input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and HSx pins

(“VBx–HSx”) occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of the high-side output, HOx, stays logic high (or “H”) because the SR flip-flop does not respond. With the HOx state being held high, the next LINx signal turns on the low-side transistor and cause a simultaneously-on condition which may result in critical damage to the IC. To protect the VBx pin against such noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC and connected between the VBx and HSx pins with a minimal length of traces.

To use an electrolytic capacitor, add a 0.01 μF to 0.1 μF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

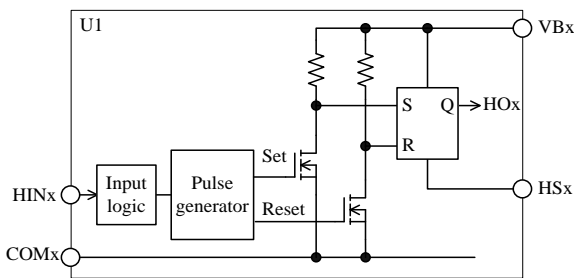


Figure 12-2. Internal Level-shifting Circuit

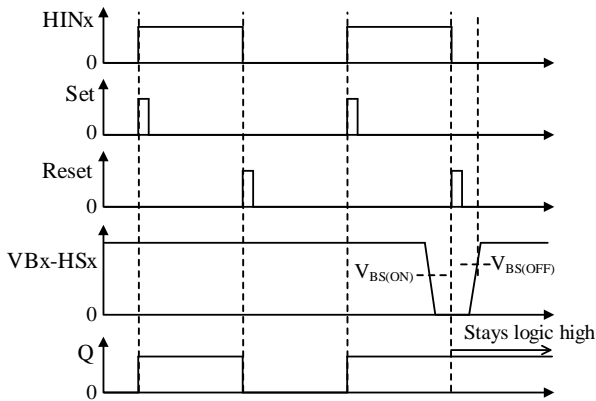


Figure 12-3. Waveforms at VBx–HSx Voltage Drop

12.2.3. HS1, HS2, and HS3

These are the inputs of the high-side floating power supplies for the individual phases. The negative side of bootstrap capacitor, C_{BOOTx}, is connected. The HS1, HS2, and HS3 pins are internally connected to the U, V, and W pins, respectively.

12.2.4. VCC1, VCC2, and VCC3

This is the logic supply pin for the built-in pre-driver IC. The VCC1, VCC2, and VCC3 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 μF to 0.1 μF ceramic capacitor, C_{VCCx}, near these pins. To prevent damage caused by surge voltages, put a 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

12.2.5. COM1, COM2, and COM3

This is the logic ground pin for the built-in pre-driver IC. For proper control, the control parts in each phase must be connected to the corresponding ground pin. The COM1, COM2, and COM3 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect these pins as close and short as possible to shunt resistors, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-4). Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the COM pin.

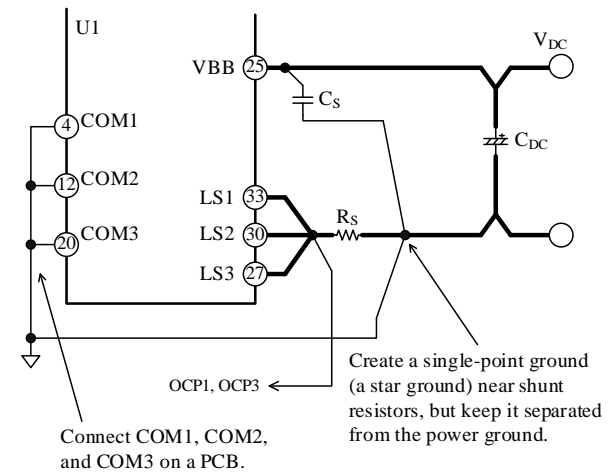


Figure 12-4. Connections to Logic Ground

12.2.6. HIN1, HIN2, and HIN3 LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller whereas the LINx pin acts as a low-side controller. Figure 12-5 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt

SCM1270MF Series

trigger circuit with a built-in 22 kΩ pull-down resistor, and its input logic is active high.

Input signals across the HIN_x-COM_x and the LIN_x-COM_x pins in each phase should be set within the ranges provided in Table 12-1, below. Note that dead time setting must be done for HIN_x and LIN_x signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures can have sufficient margins in the absolute maximum ranges specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HIN_x or LIN_x pins (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HIN_x or LIN_x pin as needed (see Figure 12-6).

Here are filter circuit constants for reference:

R_{IN1x} : 33 Ω to 100 Ω

R_{IN2x} : 1 kΩ to 10 kΩ

C_{INx} : 100 pF to 1000 pF

Extra attention should be paid when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected each other, the input voltage of the HIN_x and LIN_x pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-1. Input Signals for HIN_x and LIN_x Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	$3\text{ V} < V_{IN} < 5.5\text{ V}$	$0\text{ V} < V_{IN} < 0.5\text{ V}$
Input Pulse Width	$\geq 0.5\ \mu\text{s}$	$\geq 0.5\ \mu\text{s}$
PWM Carrier Frequency	$\leq 20\text{ kHz}$	
Dead Time	$\geq 1.5\ \mu\text{s}$	

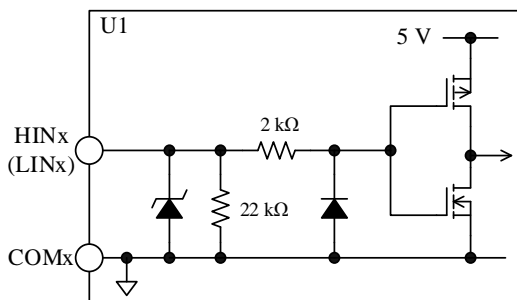


Figure 12-5. Internal Circuit Diagram of HIN_x or LIN_x Pin

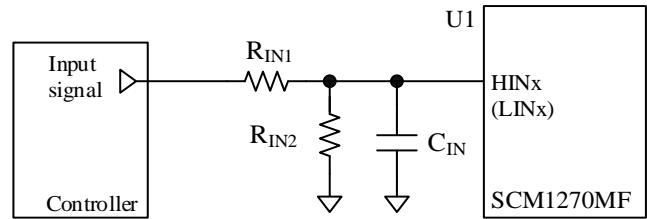


Figure 12-6. Filter Circuit for HIN_x or LIN_x Pin

12.2.7. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the VBB and COM_x pins should be set within the recommended range of the main supply voltage, V_{DC} , given in Section 2. To suppress surge voltages, put a 0.01 μF to 0.1 μF bypass capacitor, C_S , near the VBB pin and an electrolytic capacitor, C_{DC} , with a minimal length of PCB traces to the VBB pin.

12.2.8. LS1, LS2, and LS3

These are the emitter pins of the low-side IGBTs. For current detection, the LS1, LS2, and LS3 pins should be connected externally on a PCB via shunt resistors, R_S , to the COM_x pin. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS} , between the LS_x and COM_x pins in order to prevent the IC from malfunctioning.

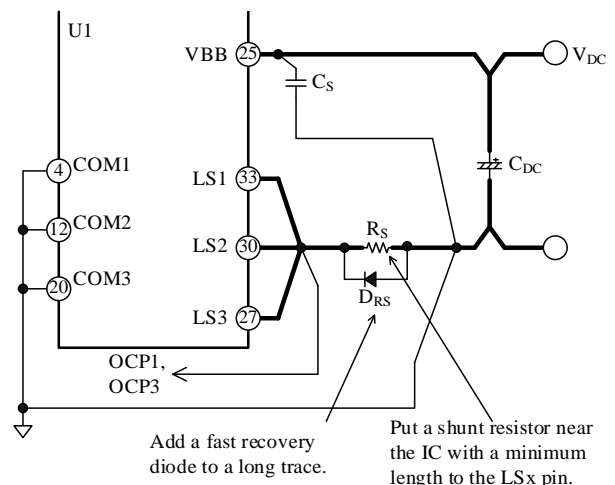


Figure 12-7. Connections to LS_x Pin

12.2.9. OCP1 and OCP3

These pins serve as the inputs of the Overcurrent Protection (OCP) for monitoring the currents going through output transistors. Section 12.4.4 provides further information about the OCP circuit configuration and its mechanism.

12.2.10. FO1 (for U-phase) and FO3 (for W-phase)

These pins operate as fault outputs and shutdown inputs for U- or W-phase. Sections 12.4.1 and 12.4.2 explain these two functions in detail, respectively.

Figure 12-8 illustrates a schematic diagram of the FOx pin and its peripheral circuit. Because of its open-drain nature, each of the FOx pins should be tied by a pull-up resistor, R_{FO} , to the external power supply. The external power supply voltage, V_{FO} , should range from 3.0 V to 5.5 V.

Figure 12-10 shows a relation between the FOx pin voltage and pull-up resistor, R_{FO} . When the pull-up resistor, R_{FO} , has a too small resistance, the FOx pin voltage at fault output becomes high due to the on-resistance of a built-in MOSFET, Q_{FO} (Figure 12-8). Therefore, it is recommended to use a 1 k Ω to 22 k Ω pull-up resistor when the low-level input threshold voltage of the microcontroller, V_{IL} , is set to 1.0 V.

To suppress noise, add a filter capacitor, C_{FO} , near the IC with minimizing a trace length between the FOx and COMx pins.

Note that, however, this additional filtering allows a delay time, $t_{D(FO)}$, to occur, as seen in Figure 12-9. The delay time, $t_{D(FO)}$, is a period of time which starts when the IC receives a fault flag turning on the internal MOSFET, Q_{FO} , and continues until when the FOx pin reaches its threshold voltage (V_{IL}) of 1.0 V or below (put simply, until the time when the IC detects a logic low state, "L"). Figure 12-11 shows how the delay time, $t_{D(FO)}$, and the noise filter capacitor, C_{FO} , are related. To avoid the repetition of Overcurrent Protection (OCP) activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_p , which occurs after the internal MOSFET (Q_{FO}) turn-on. t_p is 15 μ s where minimum values of thermal characteristics are taken into account (for more details, see Section 12.4.4). When the low-level input threshold voltage of the microcontroller, V_{IL} , is set to 1.0 V, C_{FO} should be set 1000 pF or less that V-phase delay time, $t_{D(SD)}$, at OCP activation is taken into account (see Section 12.2.11).

Motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. When putting the motor back to normal operation, you must set up a wait time of 2 seconds or longer before resuming the motor operation.

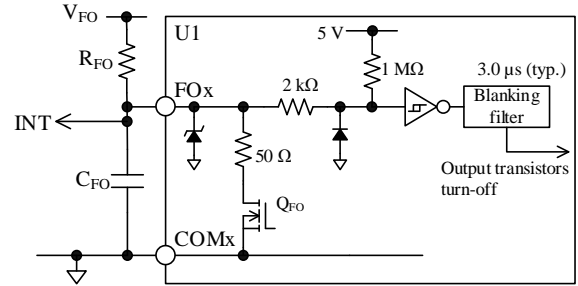


Figure 12-8. Internal Circuit Diagram of FOx Pin and Its Peripheral Circuit

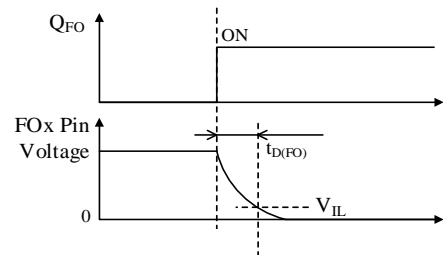


Figure 12-9. FOx Pin Delay Time, $t_{D(FO)}$

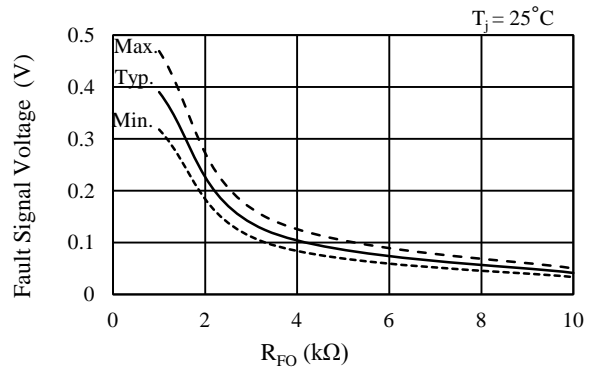


Figure 12-10. Fault Signal Voltage vs. Pull-up Resistor, R_{FO}

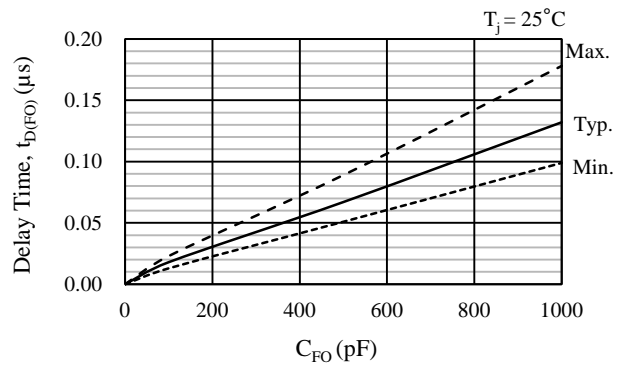


Figure 12-11. Delay Time, $t_{D(FO)}$ vs. Filter Capacitor, C_{FO}

12.2.11. SD (for V-phase)

This is the shutdown signal input pin for V-phase. Figure 12-12 illustrates a schematic diagram of the SD pin and its peripheral circuit. The SD pin is connected to the FO1 and FO3 pins in order to shutdown the V-phase output transistors by the U- and W-phase fault signals at some protections activation. When the SD pin voltage decreases to V_{IL} of 1.5 V or less, and remains in this condition for a period of the SD Pin Filtering Time ($t_{FIL(SD)}$, 300 ns) or longer, the V-phase transistors turn off.

Figure 12-14 shows a relation between $t_{D(SD)}$ and capacitance of C_{FO} . $t_{D(SD)}$ is the period until the V-phase output (HO2) turns off after internal MOSFET, Q_{FOx} , is turned on by some protections as shown in Figure 12-13.

If the period that the SD pin detects the FOx signal of the U- or W-phase OCP is too long, permanent damage to the V-phase output transistors may be caused. Thus, C_{FO} value must be set 1000 pF or less.

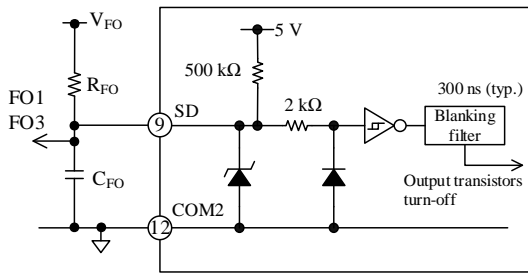


Figure 12-12. Internal Circuit Diagram of SD Pin and Its Peripheral Circuit

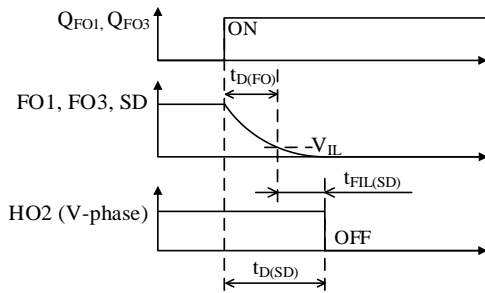


Figure 12-13. V-phase Shutdown Period, $t_{D(SD)}$

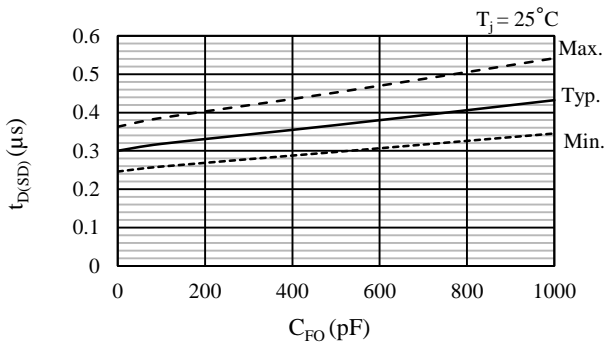


Figure 12-14. Delay Time, $t_{D(SD)}$ vs. Filter Capacitor, C_{FO}

12.2.12. VT

This pin outputs the temperature sensing voltage. The microcontroller can monitor the junction temperature of internal control IC by the VT pin (note that the sensing temperature is not the junction temperature of output transistors). For detail of Temperature Sensing Function, see Section 12.3.

12.3. Temperature Sensing Function

The microcontroller can monitor the junction temperature of internal control IC by the temperature sensing voltage that the VT pin outputs. Note that the IC does not include the protection such as the IC operation stop or the fault signal output in the over temperature status. Thus, you must set to stop the IC operation using the sensing voltage (for example, turn off the input signals).

Figure 12-15 shows the relation between VT pin voltage and temperature. Table 12-2 and Table 12-3 show the detail of variation in Figure 12-15.

Since the temperature sensing voltage may become 3.0 V or more, a clamp diode, DZ_{VT} , must be added between the power supply of the microcontroller and the VT pin to protect the microcontroller that is connected to the VT pin.

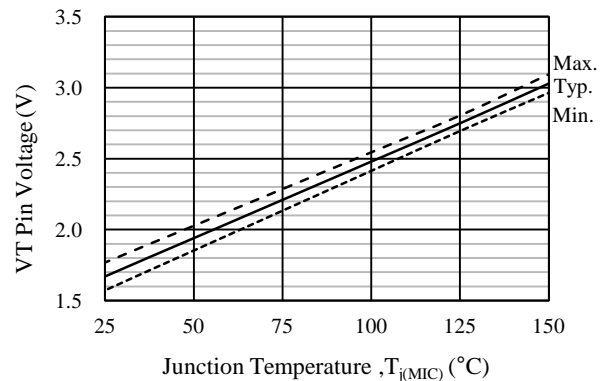


Figure 12-15. VT Pin Voltage vs. Internal Control IC Junction Temperature, $T_{j(MIC)}$

Table 12-2. $T_{j(MIC)}$ Variation of VT Pin Voltage

VT Pin Voltage	$T_{j(MIC)}$
1.95 V	$50 \pm 8^\circ\text{C}$
2.75 V	$125 \pm 5^\circ\text{C}$

Table 12-3. VT Pin Voltage Variation of $T_{j(MIC)}$

$T_{j(MIC)}$	VT Pin Voltage
50°C	$1.95 \pm 0.9\text{ V}$
125°C	$2.75 \pm 0.06\text{ V}$

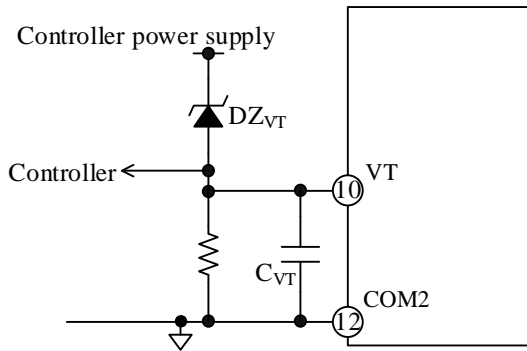


Figure 12-16. VT Pin Peripheral Circuit

12.4. Protections

This section describes the various protection circuits provided in the SCM1270MF series. The protection circuits include: the Undervoltage Lockout for power supplies (UVLO), the Simultaneous On-state prevention, and the Overcurrent Protection (OCP). In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop all operations of the three phases by receiving the fault signal. The external microcontroller can also shut down the IC operations by inputting a fault signal to the FO pin.

In the following functional descriptions, “HOx” denotes a gate input signal on the high-side transistor whereas “LOx” denotes a gate input signal on the low-side transistor (see also the diagram in Section 7).

“VBx–HSx” refers to the voltages between the VBx pin and HSx pin.

12.4.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FOx} , turns on; then the FO pin becomes logic low ($\leq 0.5\text{ V}$). The FO1, FO3, and SD pins must be all connected by external traces.

- 1) Low-side Undervoltage Lockout (UVLO_VCC)
- 2) Overcurrent Protection (OCP)
- 3) Simultaneous On-state Prevention

During the time when the FOx pin holds the logic low state, the high- and low-side transistors of each phase turn off. In normal operation, the FOx pin holds a high state and outputs a 5 V signal. The fault signal output time of the FOx pin at OCP activation is the OCP hold time (t_p) of 26 μs (typ.), fixed by a built-in feature of the IC itself (see Section 12.4.4). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the INHx and INLx pins to logic low within the predetermined OCP hold time, t_p . When putting the motor back to normal operation, you must set up a wait

time of 2 seconds or longer before resuming the motor operation.

12.4.2. Shutdown Signal Input

The FO1, FO3, and SD pins also can be the input pins of shutdown signals. When the FOx and SD pins becomes logic low, the high- and low-side transistors of each phase turn off.

The voltages and pulse widths of the shutdown signals are required to set as listed in Table 12-4.

Table 12-4. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	$3\text{ V} < V_{IN} < 5.5\text{ V}$	$0\text{ V} < V_{IN} < 0.5\text{ V}$
Input Pulse Width	$\geq 3.0\ \mu\text{s}$	$\geq 3.0\ \mu\text{s}$

FO1, FO3, and SD pins must be all connected as shown in Figure 12-17. If an abnormal condition is detected by the U- or W-phase monolithic ICs (MICx), the high- and low-side transistors of all phases turn off.

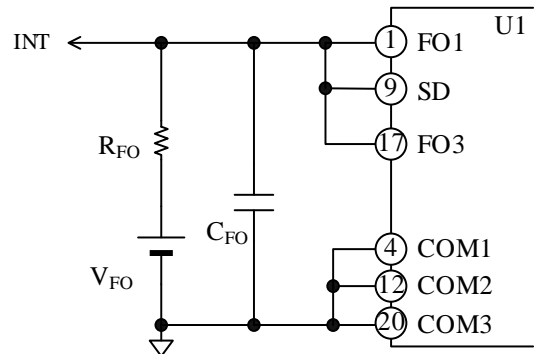


Figure 12-17. All-phase Shutdown Circuit

12.4.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltage of output transistors decreases, the steady-state power dissipation of the transistors increases. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the IC has the Undervoltage Lockout (UVLO) circuits for both of the high- and low-side power supplies in the monolithic IC (MIC).

12.4.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-18 shows operational waveforms of the undervoltage lockout operation for high-side power

supply (i.e., UVLO_VB).

When the voltage between the VBx and HSx pins (VBx–HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$, 11.0 V) or less, the UVLO_VB circuit in the corresponding phase activates and sets only the HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$, 11.5 V) or more, the IC releases the UVLO_VB condition. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release. The FOx pin does not transmit any fault signals during the UVLO_VB is in operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 μ s, in order to prevent noise-induced malfunctions.

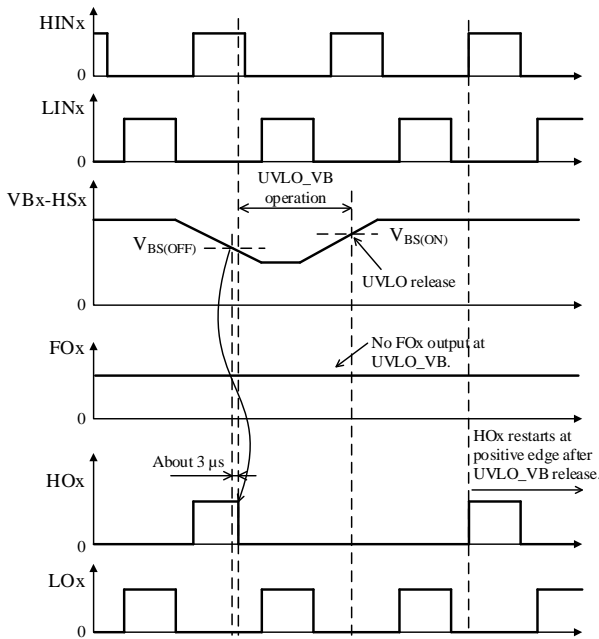


Figure 12-18. Operational Waveforms of UVLO_VB

12.4.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-19 shows operational waveforms of the undervoltage lockout operation for low-side power supply (i.e., UVLO_VCC).

The VCC1, VCC2, and VCC3 pins must be all connected by external traces on PCB.

When the VCCx pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$, 11.0 V) or less, the UVLO_VCC circuit in the corresponding phase activates and sets both of HOx and LOx signals to logic low. When the VCCx pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$, 11.5 V) or more, the IC releases the UVLO_VCC condition. Then it resumes transmitting HOx and LOx signals according to the input commands on the HINx and LINx pins. During the

UVLO_VCC operation, the FOx pin becomes logic low and sends fault signals.

In addition, the VCCx pin has an internal UVLO_VCC filter of about 3 μ s, in order to prevent noise-induced malfunctions.

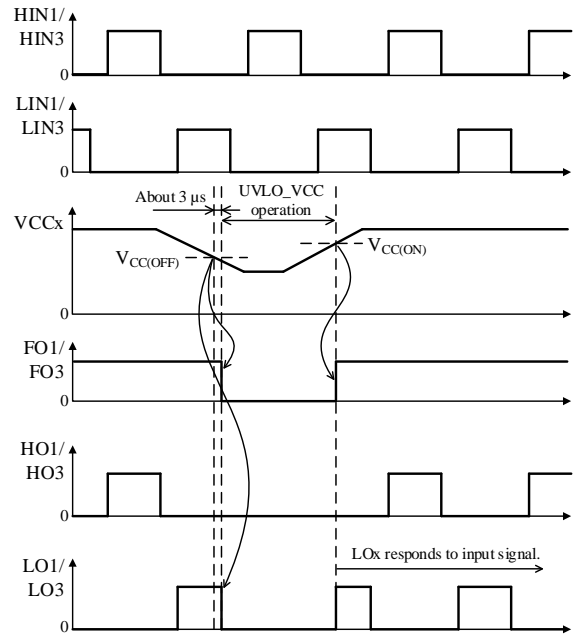


Figure 12-19. U- and W-phase Operational Waveforms of UVLO_VCC

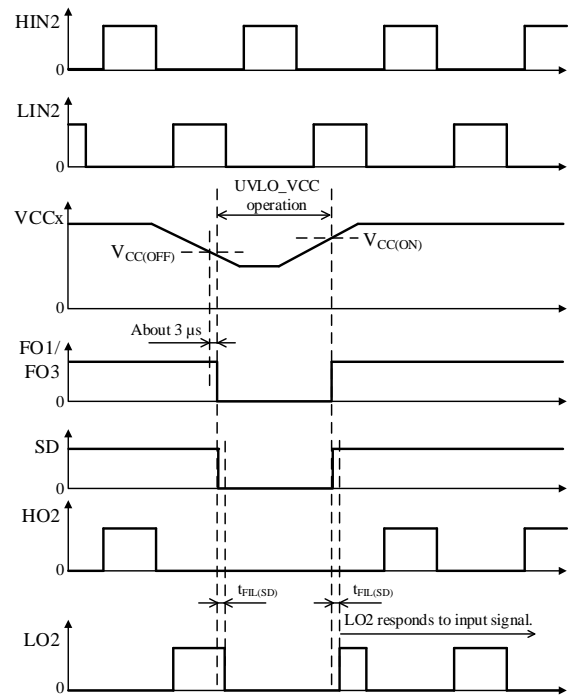


Figure 12-20. V-phase Operational Waveforms of UVLO_VCC

12.4.4. Overcurrent Protection (OCP)

The control ICs for U- and W-phase have the Overcurrent Protection (OCP) circuit. Figure 12-21 is an internal circuit diagram describing the OCP_x pin and its peripheral circuit. The OCP_x pin detects overcurrents with input voltage across an external shunt resistor, R_S. Because the OCP_x pin is internally pulled down, the OCP_x pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

Figure 12-22 shows the OCP waveforms when the OCP1 pin (U-phase) or the OCP3 pin (W-phase) detects overcurrents. When the OCP_x pin voltage increases to the Overcurrent Protection Threshold Voltage (V_{TRIP}, 0.50 V) or more, and remains in this condition for a period of the Overcurrent Protection Blanking Time (t_{BK}, 370 μs) or longer, the OCP is activated. When the internal delay time (t_{DELAY}, 0.3 μs) has elapsed after the OCP activation, the enabled OCP_x circuit then shuts off the corresponding output transistors and puts the FO_x pin into a logic low state. Then, output current decreases due to the output transistors turn-off. Even if the OCP_x pin voltage falls below V_{TRIP}, the IC holds the FO_x pin in a logic low state for a fixed OCP hold time (t_P) of 26 μs (typ.). Then, the output transistors operate according to input signals.

Because the OCP is not included the V-phase control circuit, the V-phase overcurrent signal must be input to the OCP_x pin that detects U- or W-phase OCP signal. The V-phase SD pin is connected to the U- and W-phase FO_x pins. When the OCP_x pin detects the overcurrents, the FO_x and SD pins are into logic low; and the V-phase output transistors are turned off after the SD Pin Filtering Time (t_{FIL(SD)}, 300 ns) as shown in Figure 12-23.

The V-phase turn-off delay time depends on the value of the FO pin capacitor, C_{FO}. If the delay time is too long, the output transistors may be destroyed by overcurrents. Thus, the C_{FO} value must be set 1000 pF or less.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the INH_x and INL_x pins to logic low within the predetermined OCP hold time, t_P. When putting the motor back to normal operation, you must set up a wait time of 2 seconds or longer before resuming the motor operation.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP_x pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_O and a filter capacitor, C_O) to the OCP_x pin, care should be taken in setting the time constants of R_O and C_O. The larger the time constant, the longer the time that the OCP_x pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their time constants must be set 0.82 μs or less. The filter capacitor, C_O, should also be placed near the IC, between the OCP_x and COM_x pins with a minimal length of traces.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or these traces are shorted to ground (ground fault). In case either of these pins falls into a state of ground fault, the output transistors may be destroyed.

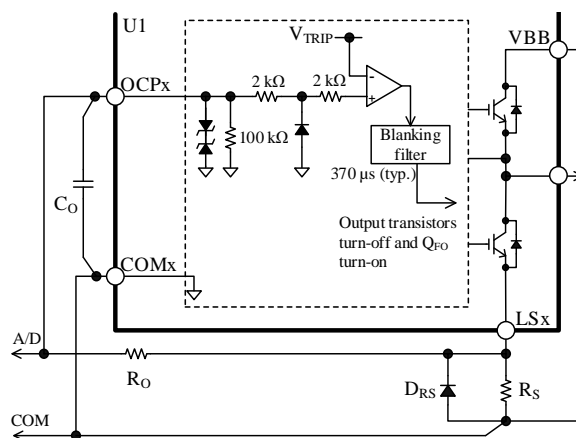


Figure 12-21. Internal Circuit Diagram of OCP_x Pin and Its Peripheral Circuit

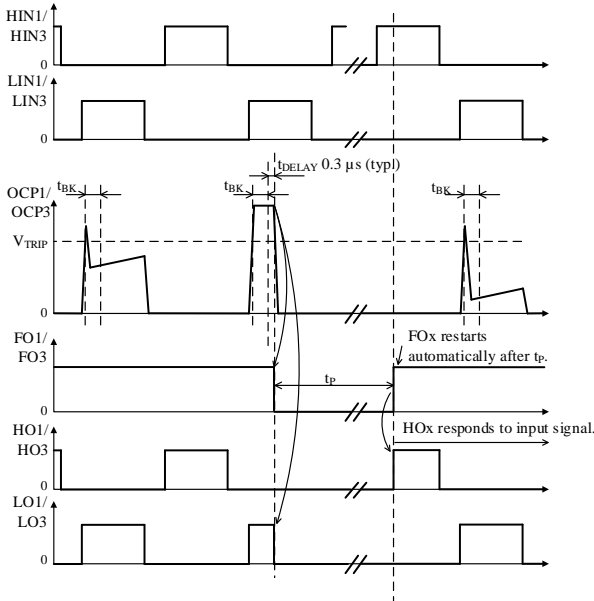


Figure 12-22. U- and W-phase OCP Operational Waveforms

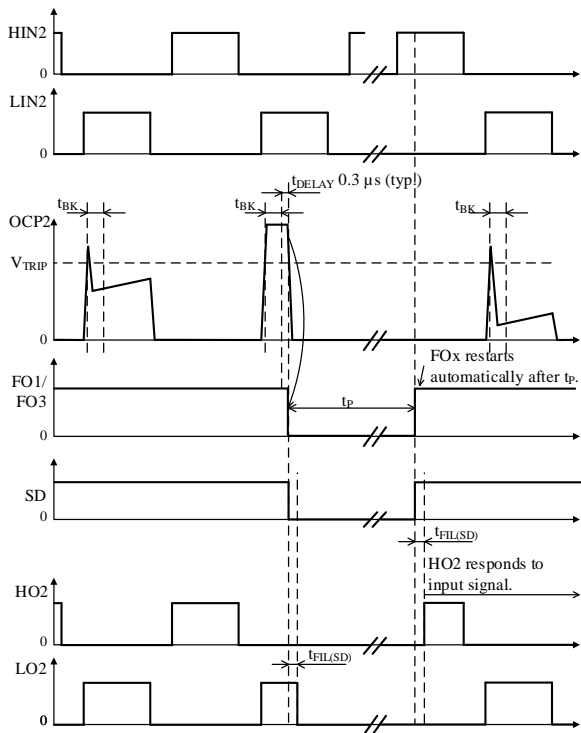


Figure 12-23. V-phase OCP Operational Waveforms

12.4.5. Simultaneous On-state Prevention

In case both of the HIN_x and LIN_x pins receive logic high signals at once, the high- and low-side transistors turn on at the same time, allowing overcurrents to pass through. As a result, the switching transistors will be destroyed. To prevent this event, the simultaneous

on-state prevention circuit is built into each of the monolithic ICs (MIC_x). Figure 12-24 shows the operational waveforms of simultaneous on-state prevention.

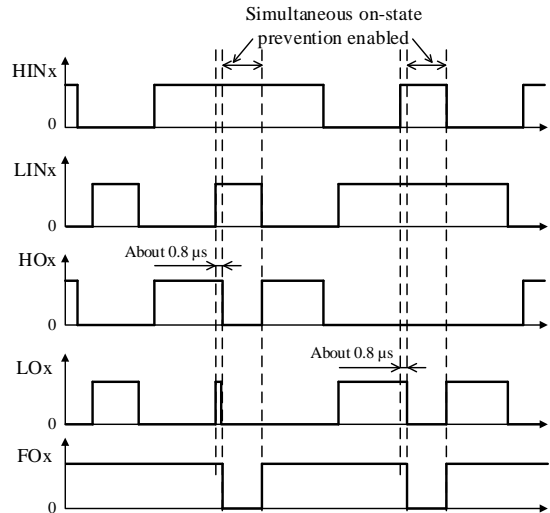


Figure 12-24. Operational Waveforms of Simultaneous On-state Prevention

When logic high signals are asserted on the HIN_x and LIN_x pins at once, as in Figure 12-24, this function gets activated and turns the high- and low-side transistors off. Then, during the function is being enabled, the FO_x pin becomes logic low and sends fault signals. After the IC comes out of the simultaneous on-state condition, “HO_x” and “LO_x” start responding in accordance with HIN_x and LIN_x input commands again.

To prevent noise-induced malfunctions, the Simultaneous On-state Prevention circuit has a filter of about 0.8 μs.

Note that this function does not have any of dead-time programming circuits. Therefore, input signals to the HIN_x and LIN_x pins must have proper dead times as defined in Section 12.2.6.

13. Design Notes

This section also employs the notation system described in the beginning of the previous section.

13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths carrying high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which carry high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

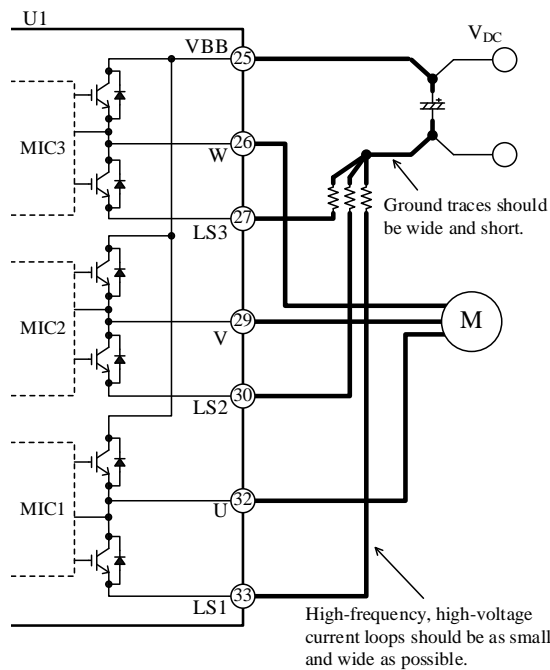


Figure 13-1. High-frequency, High-voltage Current Paths

13.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a pair of a metric screw of M3 and a plain washer of 7 mm (φ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in

Section 4.

- When mounting a heatsink, it is recommended to use silicone greases. If a thermally-conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, thorough evaluations should be conducted before using these materials.
- When applying a silicone grease, make sure that there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
 - Grease thickness: 100 μm
 - Heatsink flatness: ±100 μm
 - Apply a silicone grease within the area indicated in Figure 13-2, below.

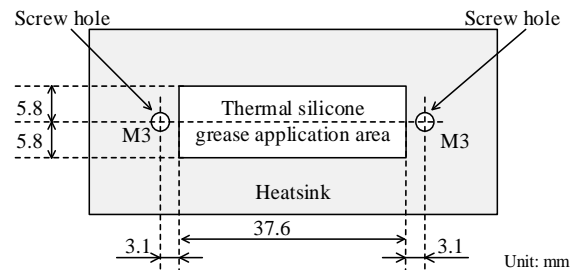


Figure 13-2. Reference Application Area for Thermal Silicone Grease

13.3. Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter of each transistor should have the same potential. Moreover, care should be taken because the collectors of the high-side transistors are all internally connected to the VBB pin. The output (U, V, and W) pins are connected to the emitters of the corresponding high-side transistors whereas the LSx pins are connected to the emitters of the low-side transistors. The gates of the high-side transistors are pulled down to the corresponding output (U, V, and W) pins; similarly, the gates of the low-side transistors are pulled down to the COMx pins. When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that all of the output (U, V, and W), LSx, and COM pins must be appropriately connected. Otherwise the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{IH}) in the U-phase whereas Figure 13-4 shows the low-side transistor (Q_{IL}) in the U-phase. And all the pins that are

not represented in these figures are open. Before conducting a measurement, be sure to isolate the ground of the to-be-measured phase from those of other two phases not to be measured. Then, in each of the two phases, which are separated not to be measured, connect the LSx and COMx pins each other at the same potential, and leave them unused and floated.

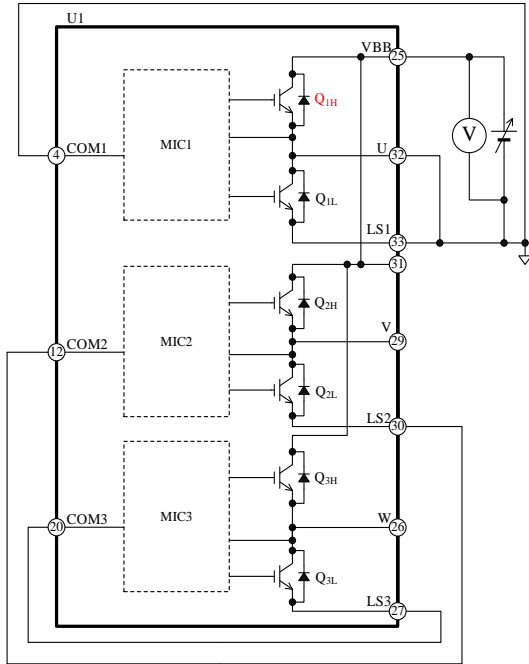


Figure 13-3. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

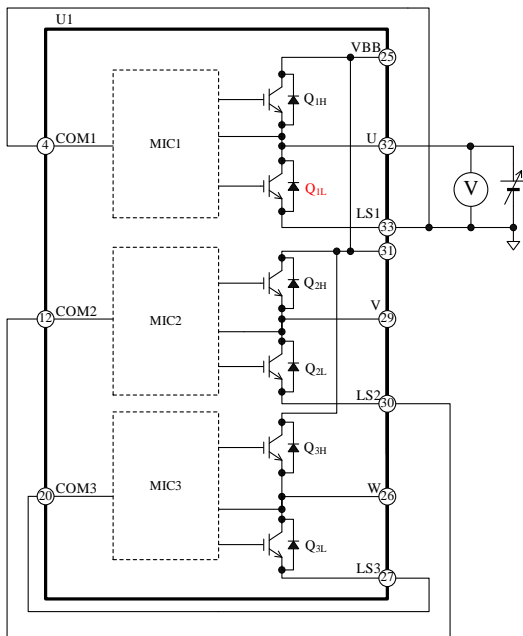


Figure 13-4. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

14. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate junction temperature. Note that the descriptions listed here are applicable to the SCM1200MF series, which is controlled by a 3-phase sine-wave PWM driving strategy. Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{sw}. The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0025: SCM1200MF Series Calculation Tool http://www.semicon.sanken-ele.co.jp/en/calc-tool/scm12xxmf_caltool_en.html

14.1. IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the V_{CE(SAT)} vs. I_C curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-1, linear approximations at a range the I_C is actually used are obtained by: V_{CE(SAT)} = α × I_C + β. The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi} \int_0^\pi V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2} \alpha \left(\frac{1}{2} + \frac{4}{3\pi} M \times \cos \theta \right) I_M^2 + \frac{\sqrt{2}}{\pi} \beta \left(\frac{1}{2} + \frac{\pi}{8} M \times \cos \theta \right) I_M \quad (4)$$

Where:

V_{CE(SAT)} is the collector-to-emitter saturation voltage of the IGBT in V,

I_C is the collector current of the IGBT in A,

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2}$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current in A,

α is the slope of the linear approximation in the V_{CE(SAT)} vs. I_C curve, and

β is the intercept of the linear approximation in the V_{CE(SAT)} vs. I_C curve.

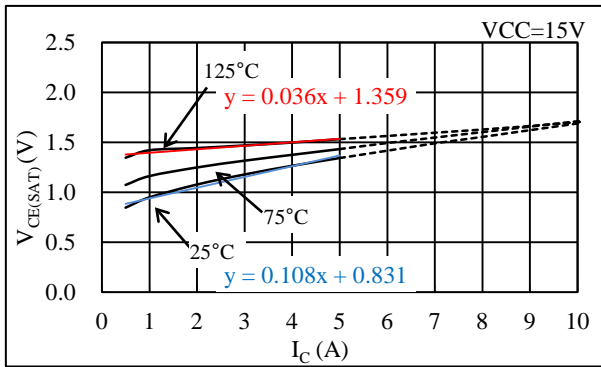


Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C Curve

14.2. IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW} , can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300} \quad (5)$$

Where:

- f_C is the PWM carrier frequency in Hz,
- V_{DC} is the main power supply voltage in V (i.e., the VBB pin input voltage), and
- α_E is the slope of the switching loss curve (see Section 15.3.2).

14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, T_j , can be estimated with Equation (6):

$$T_j = R_{(j-c)Q} \times (P_{ON} + P_{SW}) + T_C \quad (6)$$

Where:

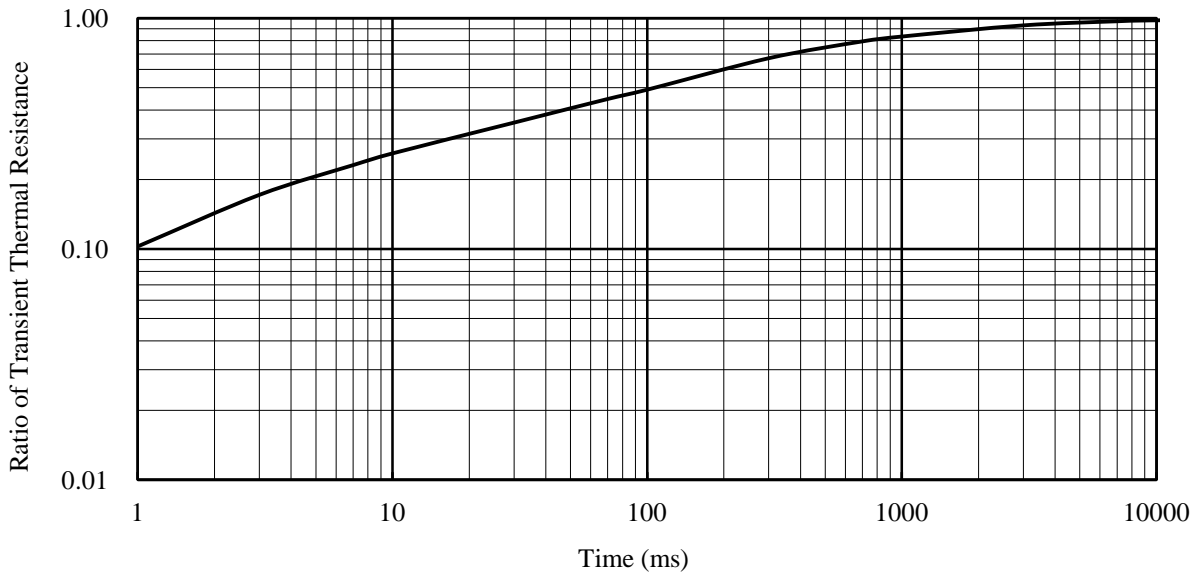
- $R_{(j-c)Q}$ is the junction-to-case thermal resistance per IGBT in $^{\circ}C/W$, and
- T_C is the case temperature in $^{\circ}C$, measured at the point defined in Figure 3-1.

15. Performance Curves

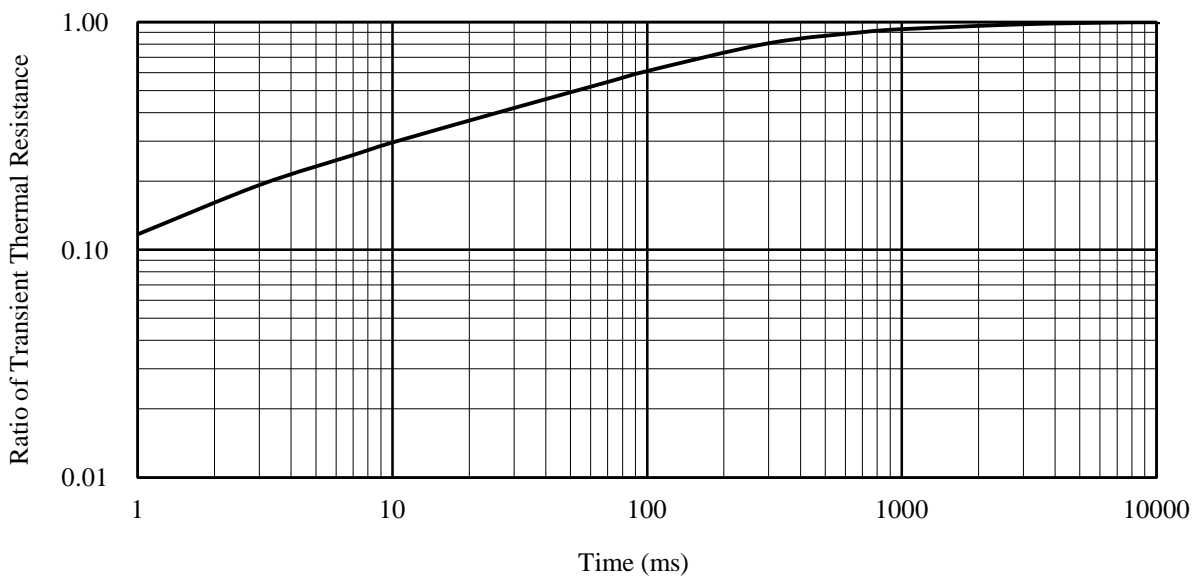
15.1. Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

15.1.1. SCM1271MF



15.1.2. SCM1272MF, SCM1274MF, and SCM1276MF



15.2. Performance Curves of Control Parts

Figure 15-1 to Figure 15-23 provide performance curves of the control parts integrated in the SCM1200MF series, including variety-dependent characteristics and thermal characteristics. T_j represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-1	Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C
Figure 15-2	Logic Supply Current in 3-phase Operation, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 15-3	Logic Supply Current in 1-phase Operation ($HINx = 0$ V), I_{BS} vs. T_C
Figure 15-4	Logic Supply Current in 1-phase Operation ($HINx = 5$ V), I_{BS} vs. T_C
Figure 15-5	Logic Supply Current in 1-phase Operation ($HINx = 0$ V), I_{BS} vs. VBx Pin Voltage, V_B
Figure 15-6	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-7	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-8	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-9	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-10	UVLO_VB Filtering Time vs. T_C
Figure 15-11	UVLO_VCC Filtering Time vs. T_C
Figure 15-12	Input Current at High Level ($HINx$ or $LINx$), I_{IN} vs. T_C
Figure 15-13	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-14	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 15-15	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-16	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-17	FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C
Figure 15-18	Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-19	Blanking Time, t_{BK} + Propagation Delay, t_{DELAY} vs. T_C
Figure 15-20	Overcurrent Protection Hold Time, t_P vs. T_C
Figure 15-21	Filtering Time of Simultaneous On-state Prevention vs. T_C
Figure 15-22	SD Pin Filtering Time, $t_{FIL(SD)}$ vs. T_C
Figure 15-23	V-phase Shutdown Period, $t_{D(SD)}$ vs. T_C

SCM1270MF Series

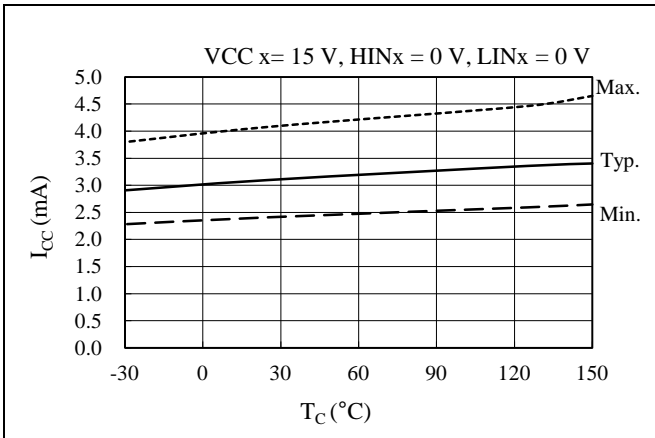


Figure 15-1. Logic Supply Current in 3-phase Operation, I_{CC} vs. T_C

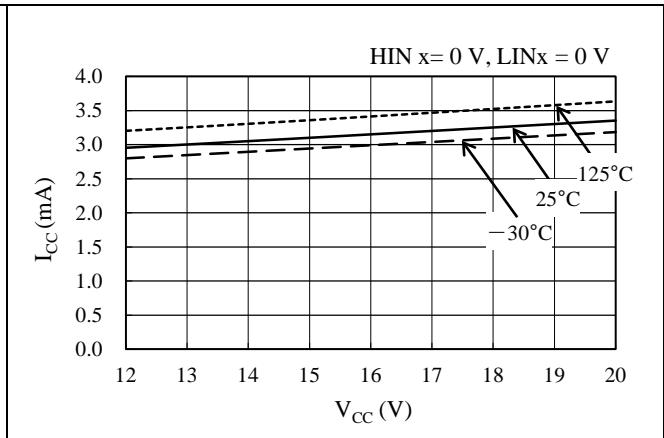


Figure 15-2. Logic Supply Current in 3-phase Operation, I_{CC} vs. V_{CCx} Pin Voltage, V_{CC}

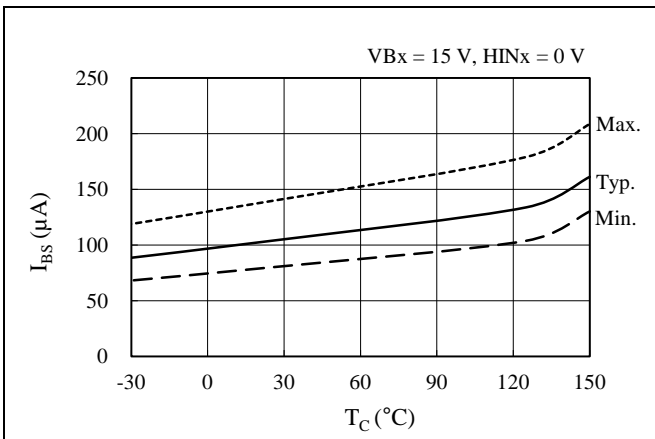


Figure 15-3. Logic Supply Current in 1-phase Operation ($HINx = 0 V$), I_{BS} vs. T_C

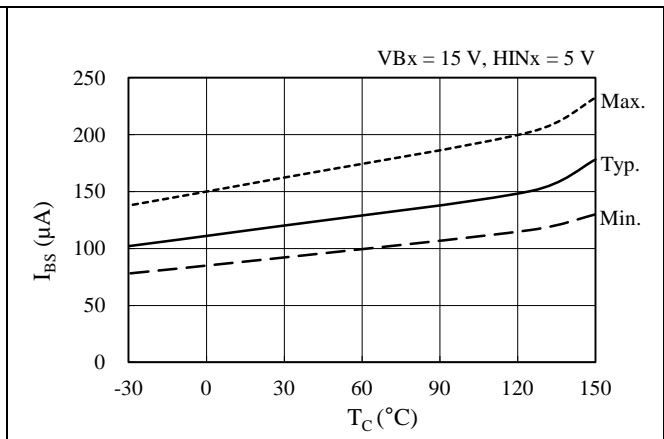


Figure 15-4. Logic Supply Current in 1-phase Operation ($HINx = 5 V$), I_{BS} vs. T_C

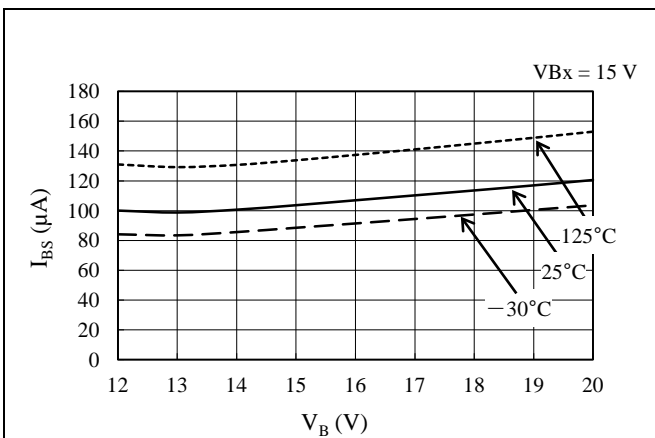


Figure 15-5. Logic Supply Current in 1-phase Operation ($HINx = 0 V$), I_{BS} vs. V_{Bx} Pin Voltage, V_B

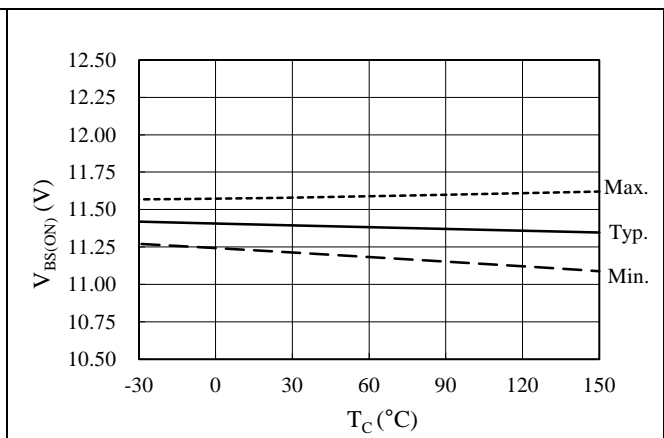


Figure 15-6. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

SCM1270MF Series

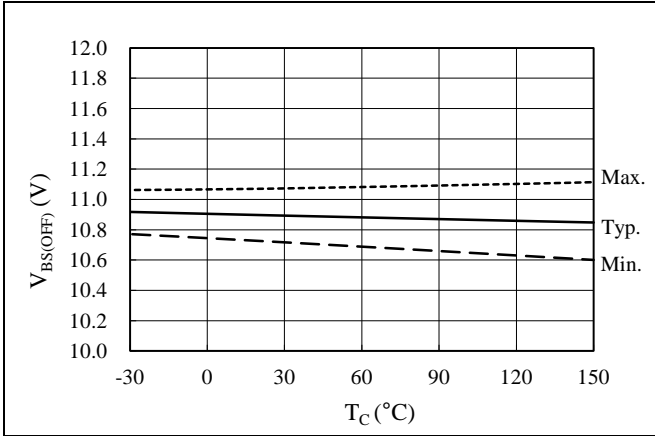


Figure 15-7. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

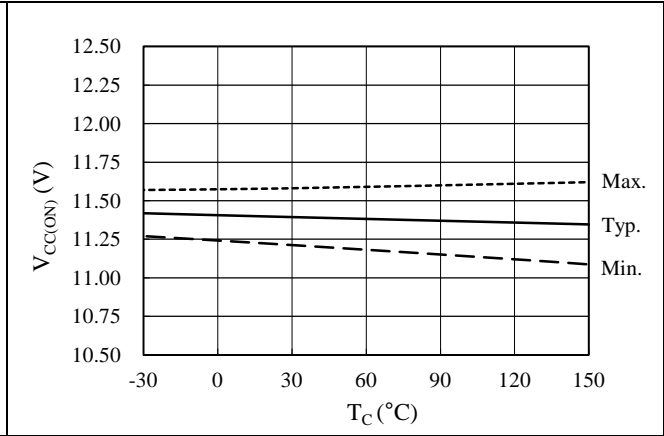


Figure 15-8. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

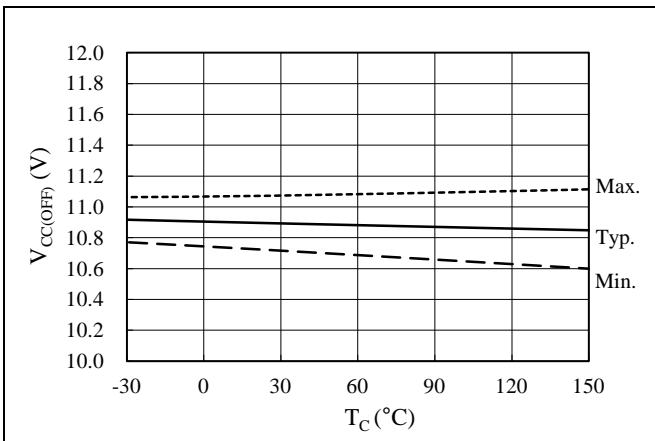


Figure 15-9. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

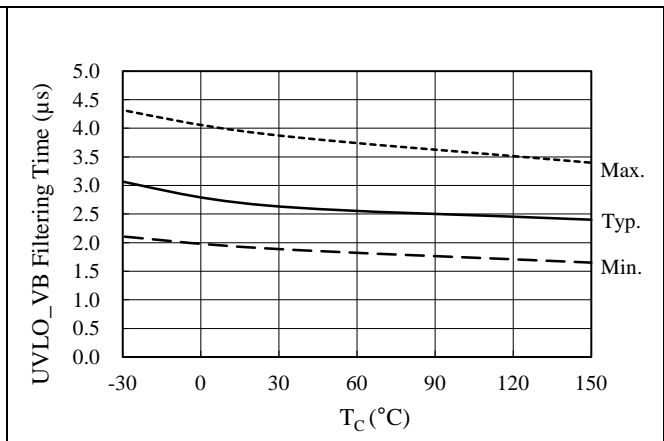


Figure 15-10. UVLO_VB Filtering Time vs. T_C

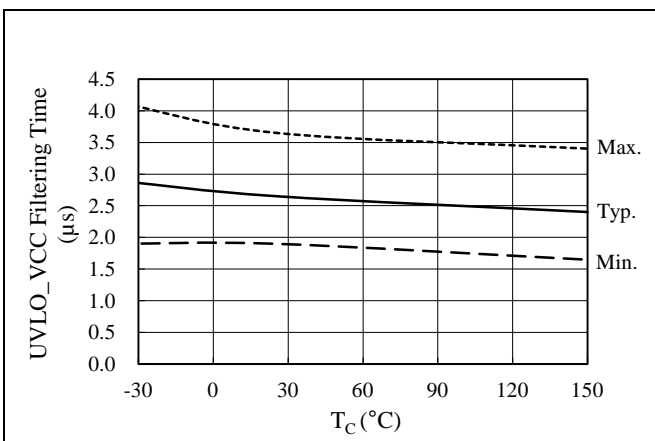


Figure 15-11. UVLO_VCC Filtering Time vs. T_C

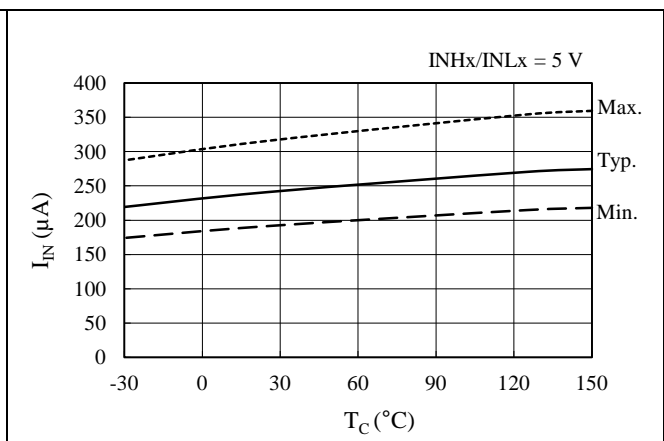


Figure 15-12. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

SCM1270MF Series

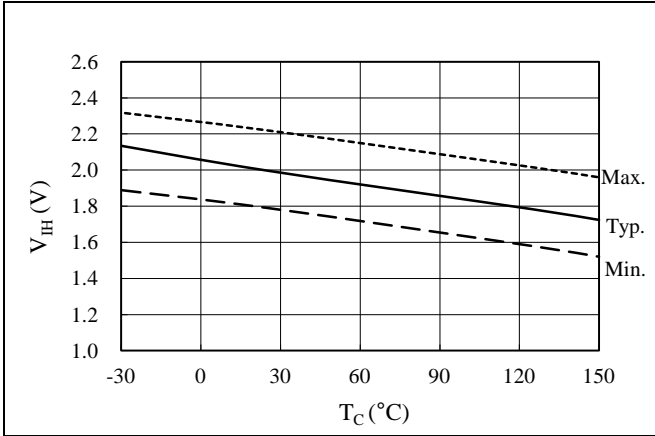


Figure 15-13. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

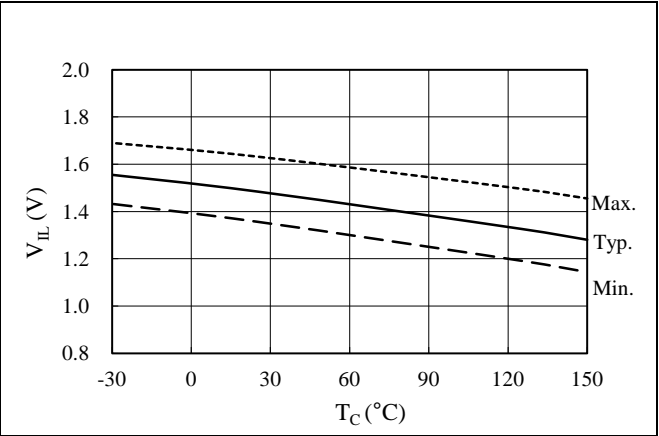


Figure 15-14. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

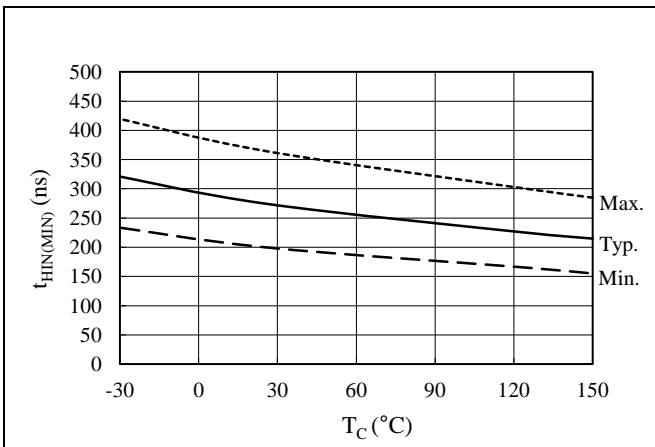


Figure 15-15. Minimum Transmittable Pulse Width for High-side Switching, $t_{HI(MIN)}$ vs. T_C

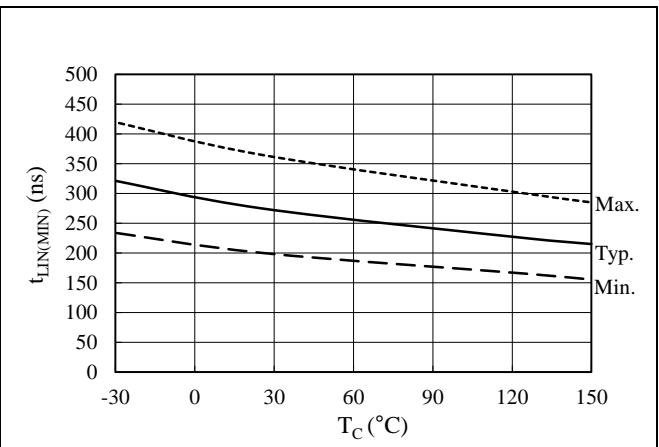


Figure 15-16. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LI(MIN)}$ vs. T_C

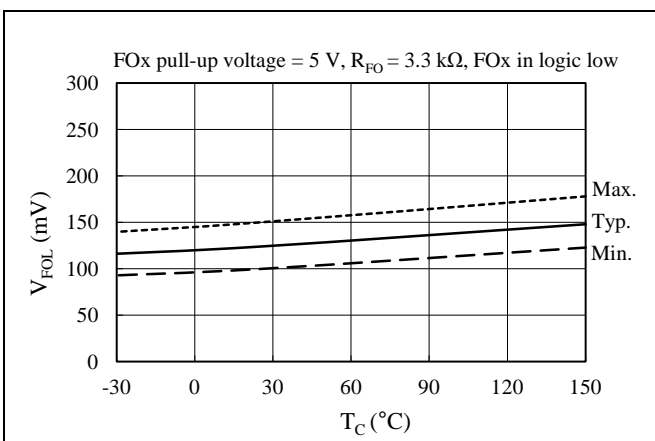


Figure 15-17. FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C

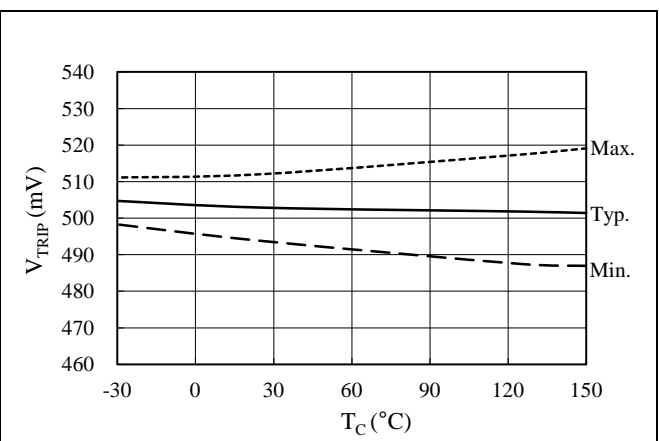


Figure 15-18. Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C

SCM1270MF Series

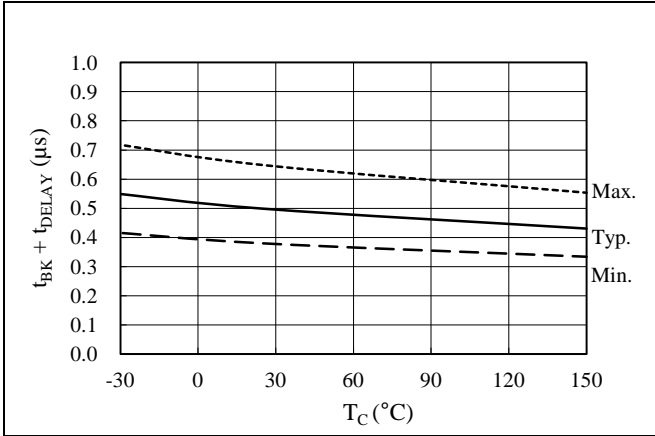


Figure 15-19. Blanking Time, t_{BK} + Propagation Delay, t_{DELAY} vs. T_C

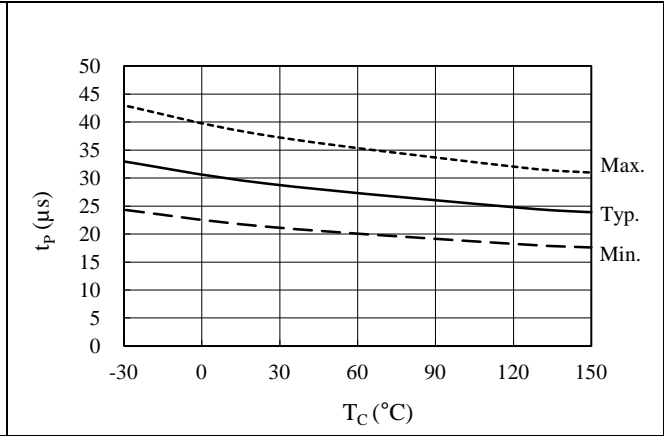


Figure 15-20. Overcurrent Protection Hold Time, t_P vs. T_C

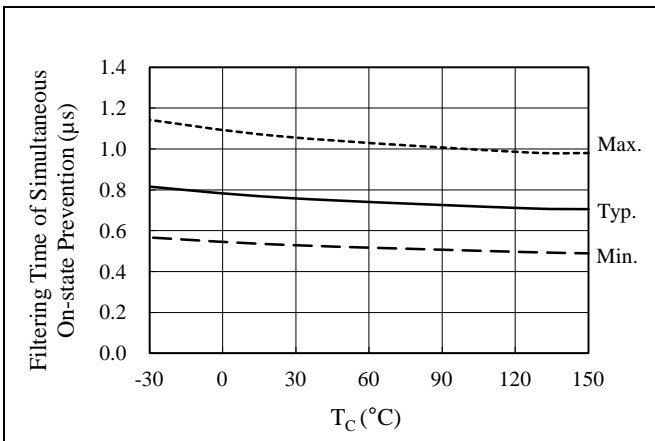


Figure 15-21. Filtering Time of Simultaneous On-state Prevention vs. T_C

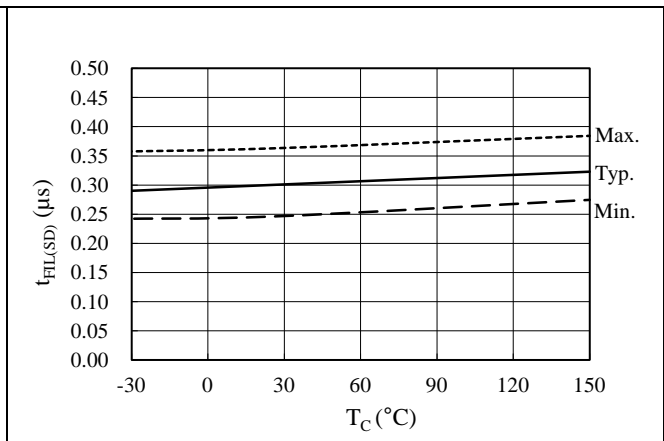


Figure 15-22. SD Pin Filtering Time, $t_{FIL(SD)}$ vs. T_C

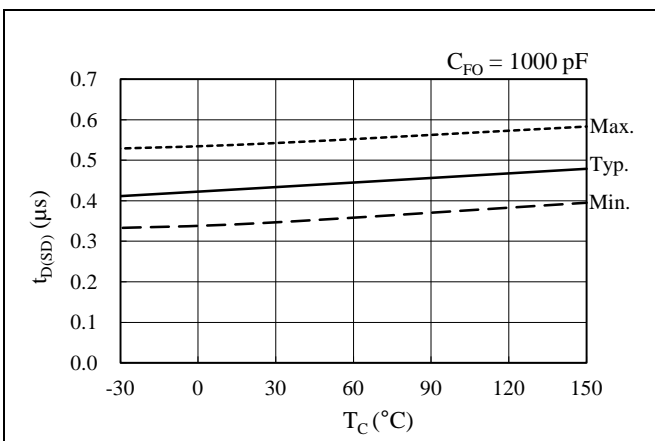


Figure 15-23. V-phase Shutdown Period, $t_{D(SD)}$ vs. T_C

SCM1270MF Series

15.3. Performance Curves of Output Parts

15.3.1. Output Transistor Performance Curves

15.3.1.1. SCM1271MF

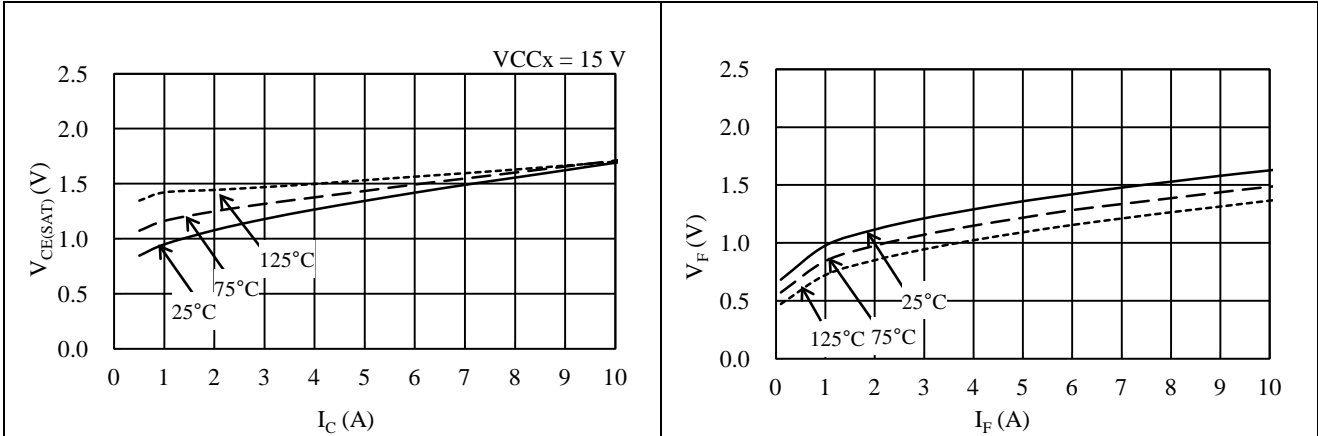


Figure 15-24. IGBT $V_{CE(SAT)}$ vs. I_C

Figure 15-25. Freewheeling Diode V_F vs. I_F

15.3.1.2. SCM1272MF

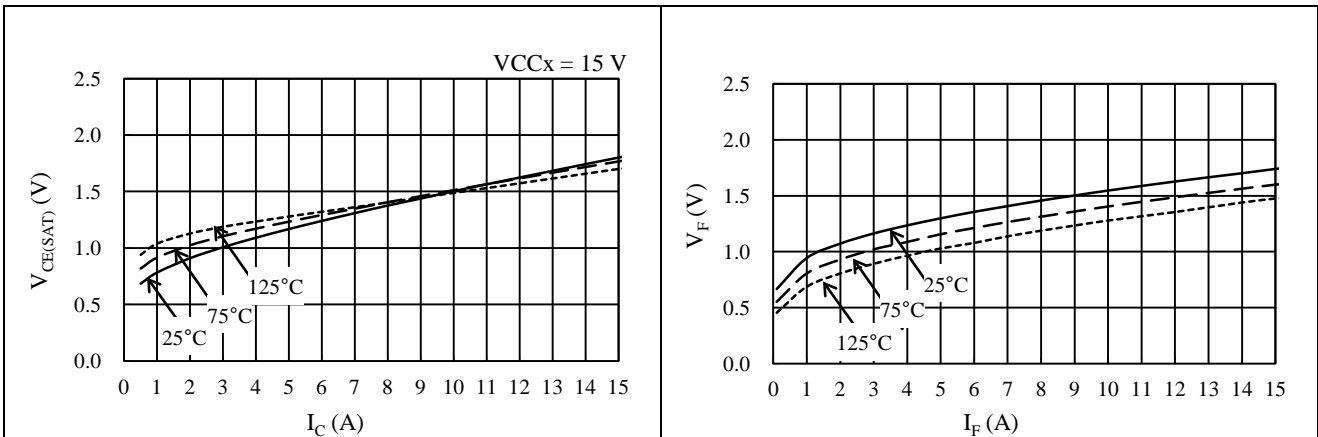


Figure 15-26. IGBT $V_{CE(SAT)}$ vs. I_C

Figure 15-27. Freewheeling Diode V_F vs. I_F

SCM1270MF Series

15.3.1.3. SCM1274MF

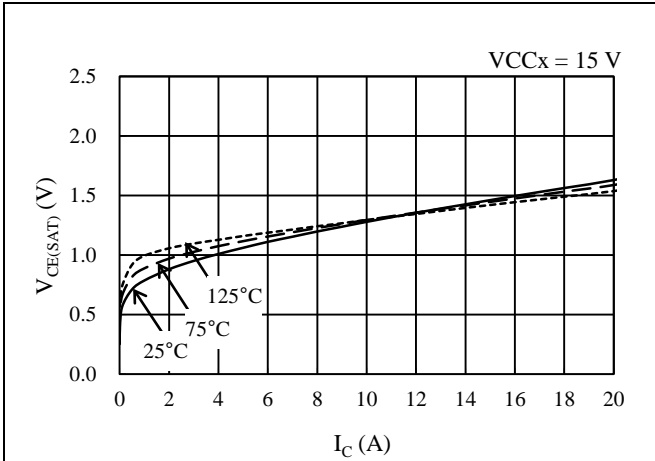


Figure 15-28. IGBT $V_{CE(SAT)}$ vs. I_C

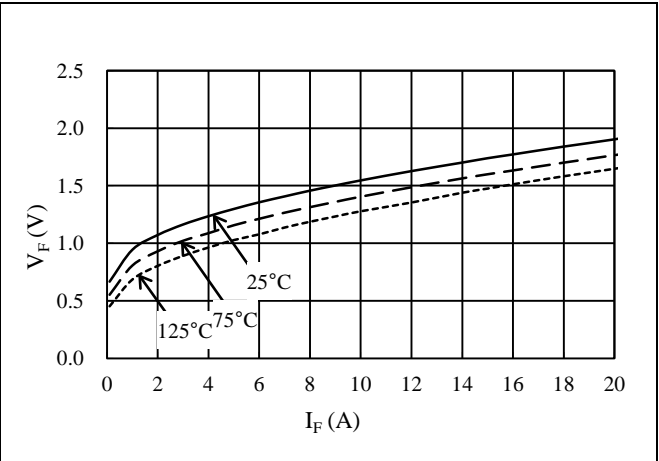


Figure 15-29. Freewheeling Diode V_F vs. I_F

15.3.1.4. SCM1276MF

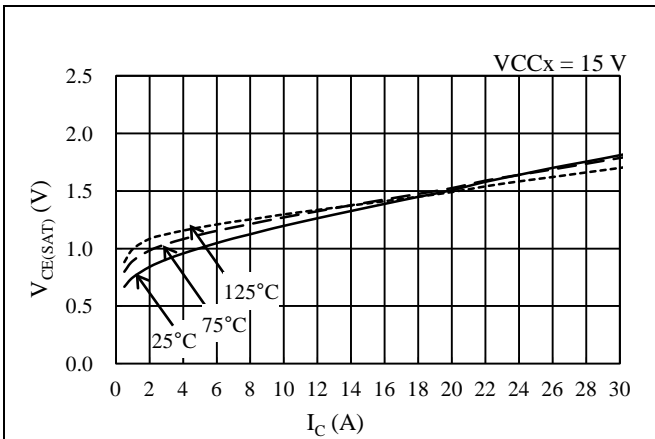


Figure 15-30. IGBT $V_{CE(SAT)}$ vs. I_C

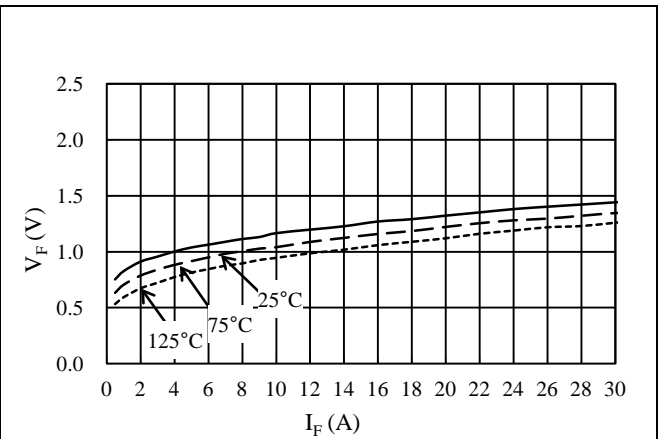


Figure 15-31. Freewheeling Diode V_F vs. I_F

SCM1270MF Series

15.3.2. Switching Losses

Conditions: $V_{BB} = 300\text{ V}$, half-bridge circuit with inductive load.

15.3.2.1. SCM1271MF

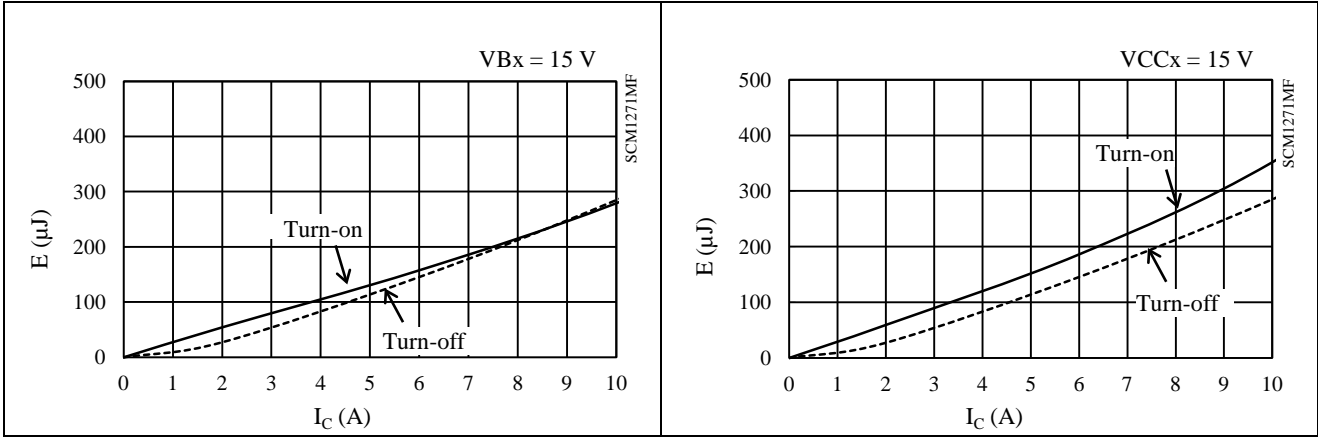


Figure 15-32. High-side Switching Loss ($T_j = 25\text{ °C}$)

Figure 15-33. Low-side Switching Loss ($T_j = 25\text{ °C}$)

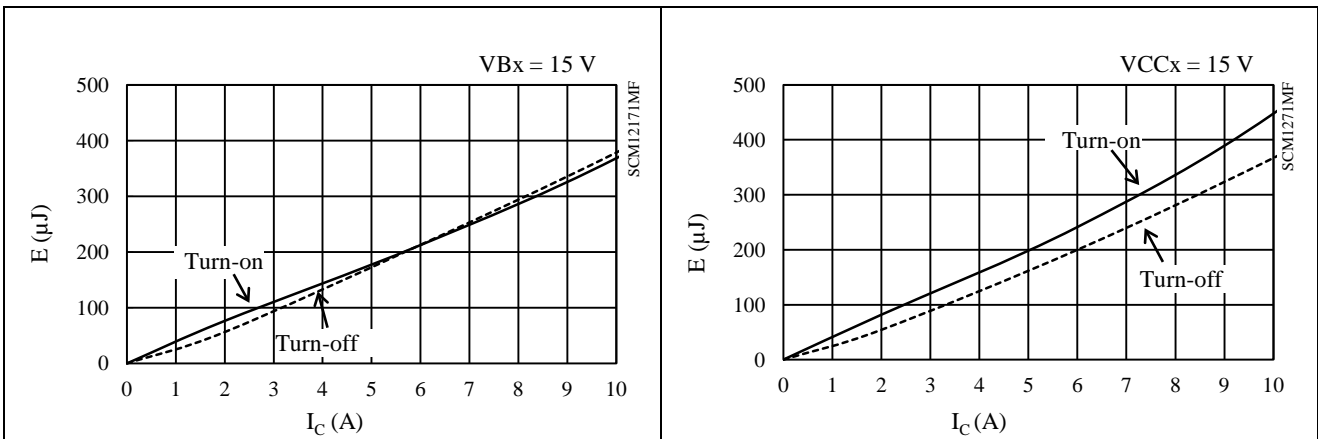


Figure 15-34. High-side Switching Loss ($T_j = 125\text{ °C}$)

Figure 15-35. Low-side Switching Loss ($T_j = 125\text{ °C}$)

SCM1270MF Series

15.3.2.2. SCM1272MF

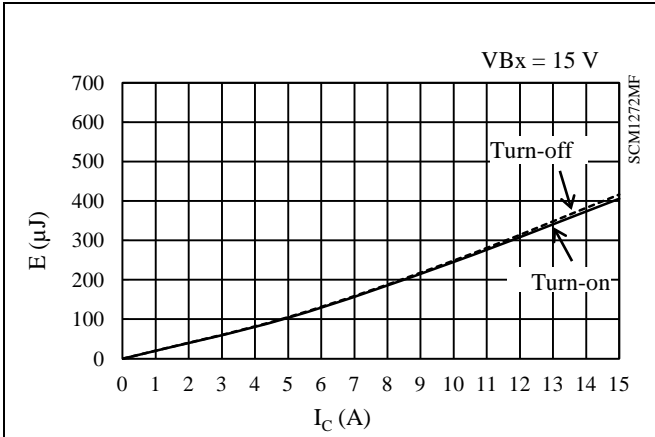


Figure 15-36. High-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

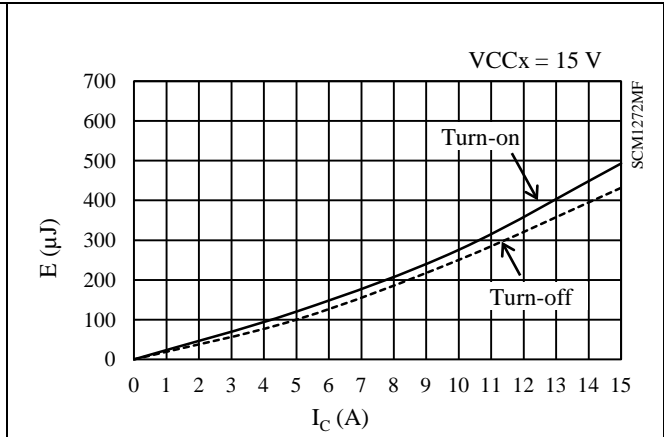


Figure 15-37. Low-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

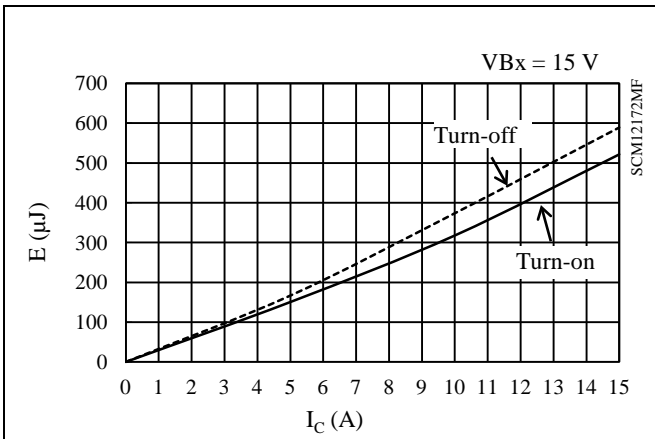


Figure 15-38. High-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

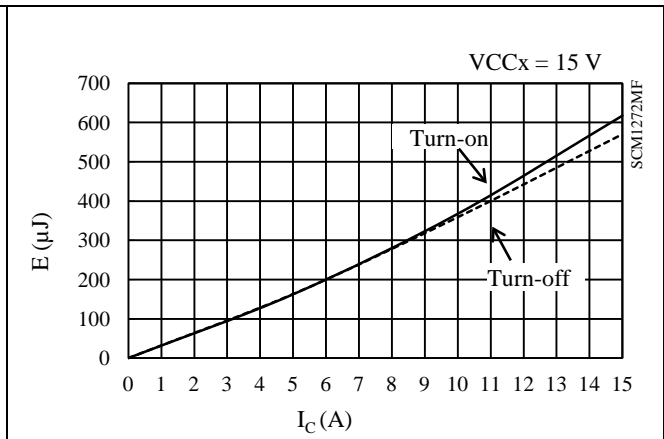


Figure 15-39. Low-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

15.3.2.3. SCM1274MF

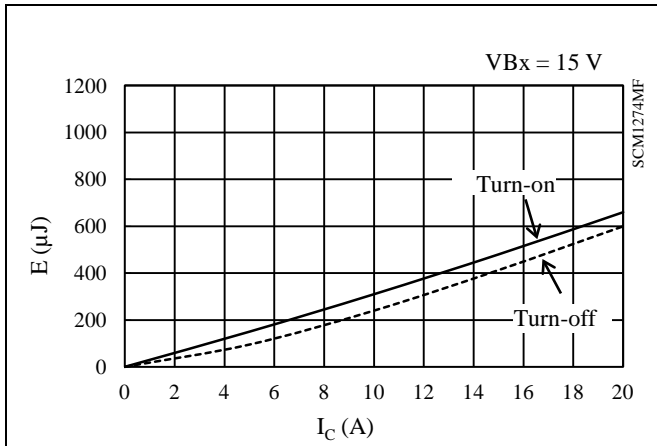


Figure 15-40. High-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

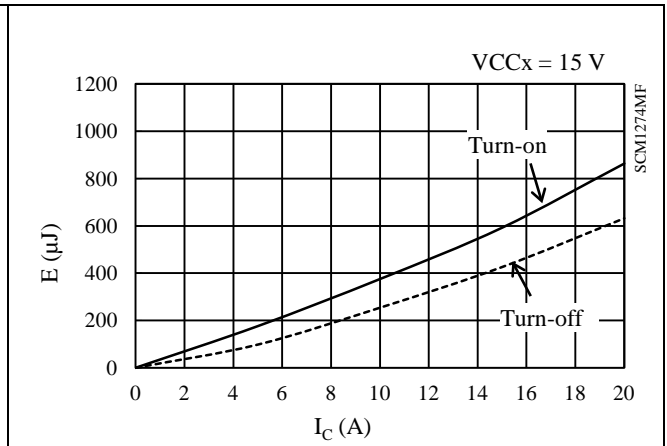


Figure 15-41. Low-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

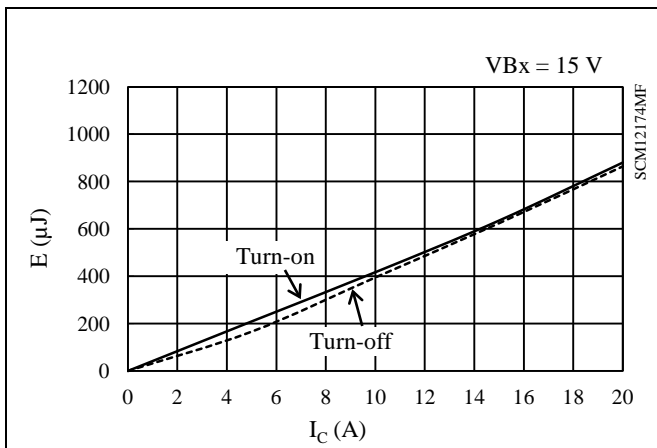


Figure 15-42. High-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

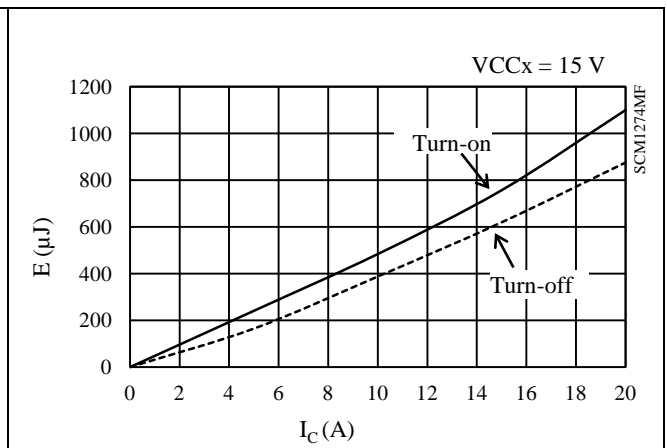


Figure 15-43. Low-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

SCM1270MF Series

15.3.2.4. SCM1276MF

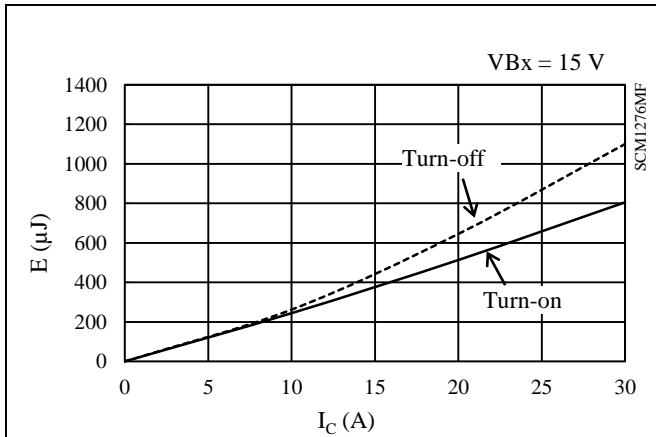


Figure 15-44. High-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

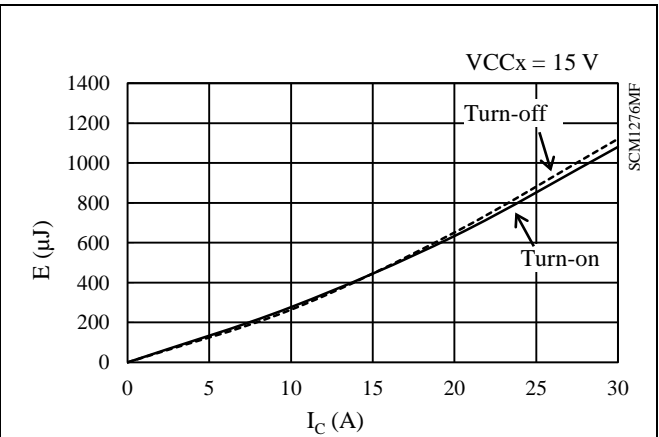


Figure 15-45. Low-side Switching Loss ($T_j = 25\text{ }^\circ\text{C}$)

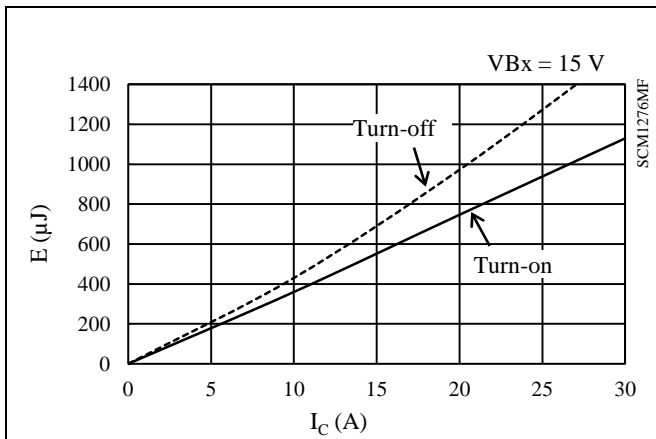


Figure 15-46. High-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

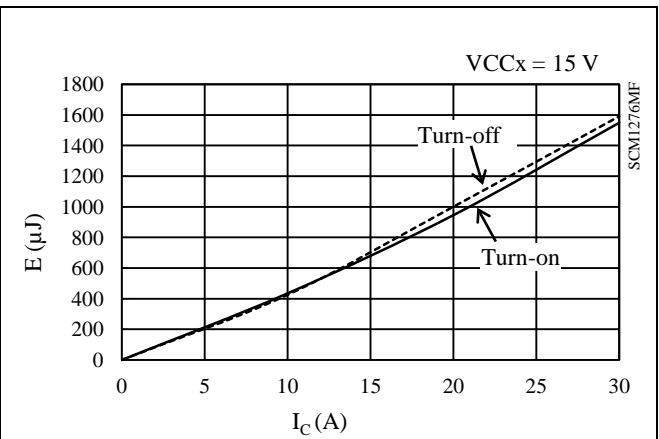


Figure 15-47. Low-side Switching Loss ($T_j = 125\text{ }^\circ\text{C}$)

15.4. Allowable Effective Current Curves

The following curves represent allowable effective currents in sine-wave driving under a 3-phase PWM system. All the values listed in this section, including $V_{CE(SAT)}$ of output transistors and switching losses, are typical values.

Operating conditions: VBB pin input voltage, $V_{DC} = 300\text{ V}$; VCC pin input voltage, $V_{CC} = 15\text{ V}$; modulation index, $M = 0.9$; motor power factor, $\cos\theta = 0.8$; junction temperature, $T_j = 150\text{ }^\circ\text{C}$.

15.4.1. SCM1271MF

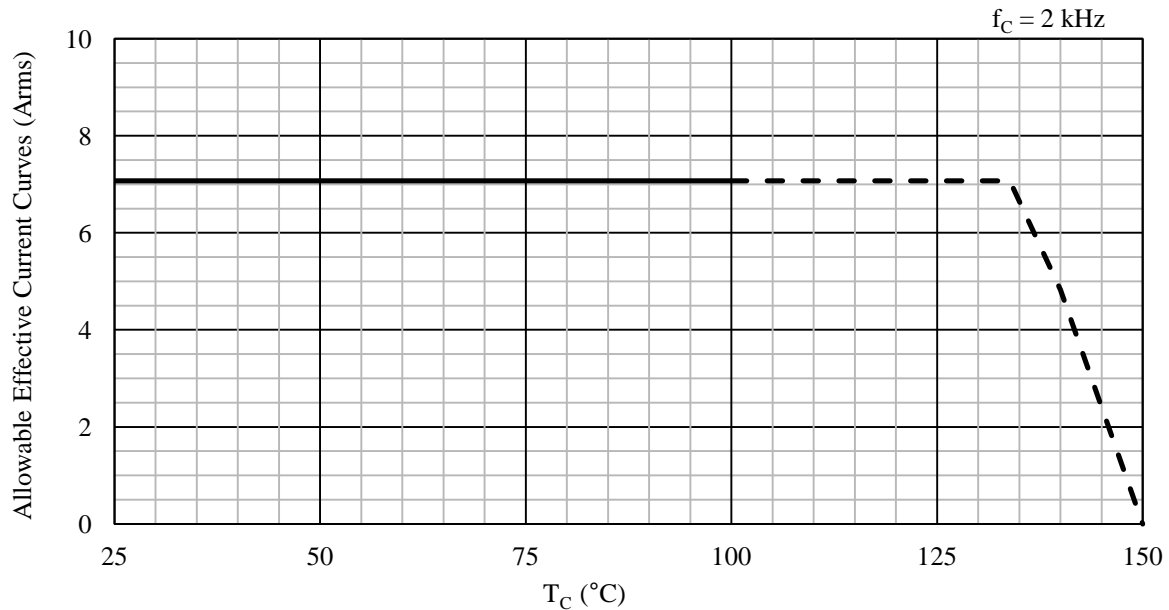


Figure 15-48. SCM1271MF Allowable Effective Current ($f_c = 2\text{ kHz}$)

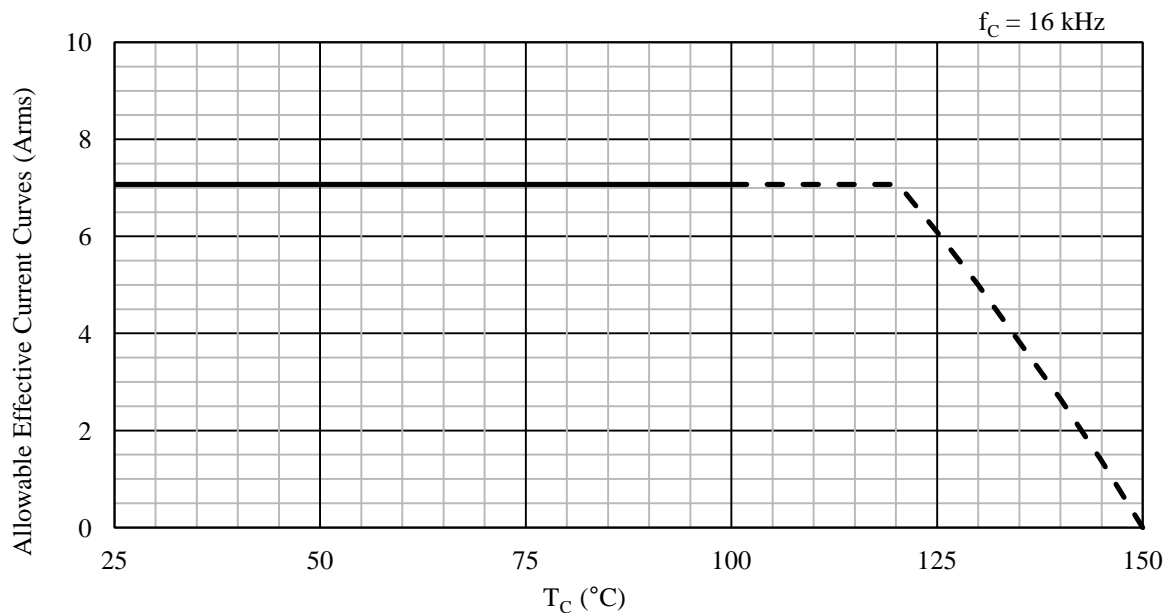


Figure 15-49. SCM1271MF Allowable Effective Current ($f_c = 16\text{ kHz}$)

15.4.2. SCM1272MF

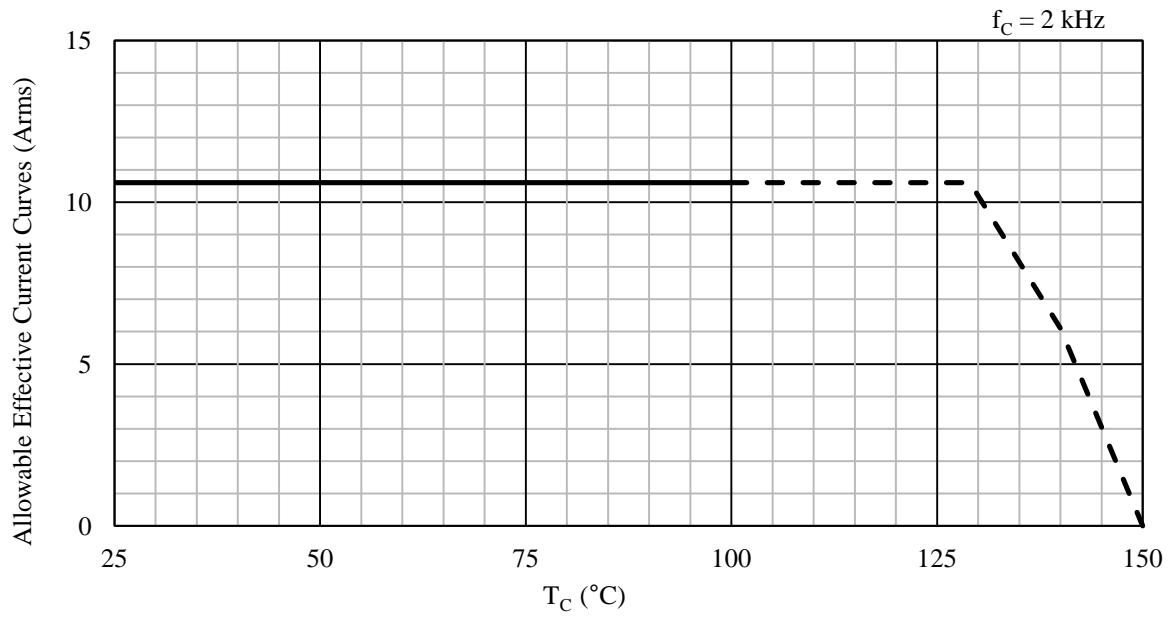


Figure 15-50. SCM1272MF Allowable Effective Current ($f_c = 2$ kHz)

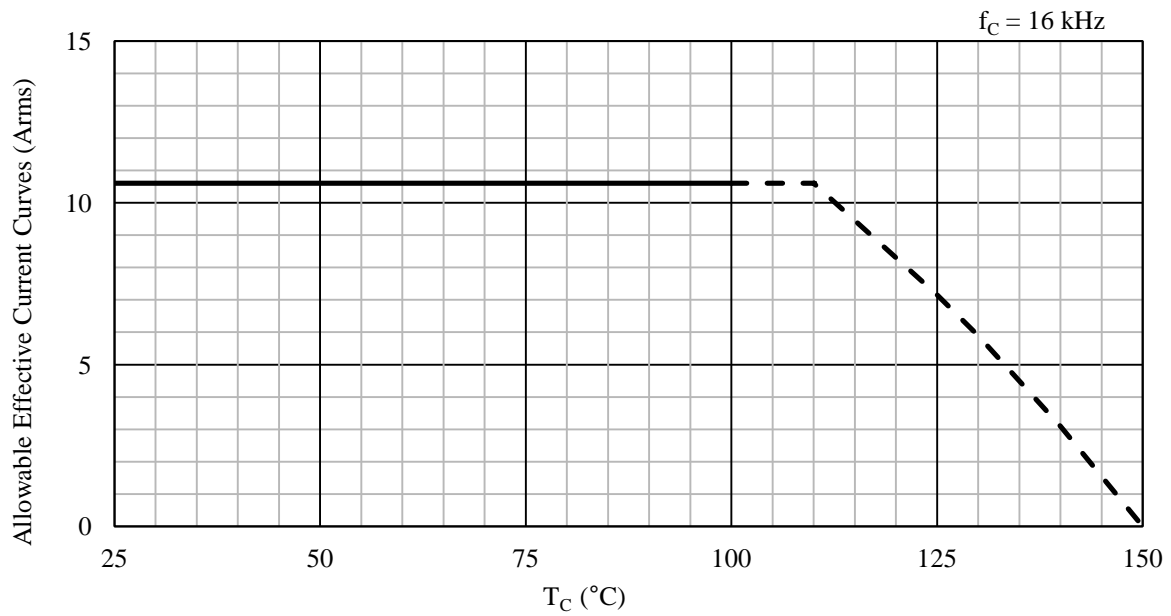


Figure 15-51. SCM1272MF Allowable Effective Current ($f_c = 16$ kHz)

15.4.3. SCM1274MF

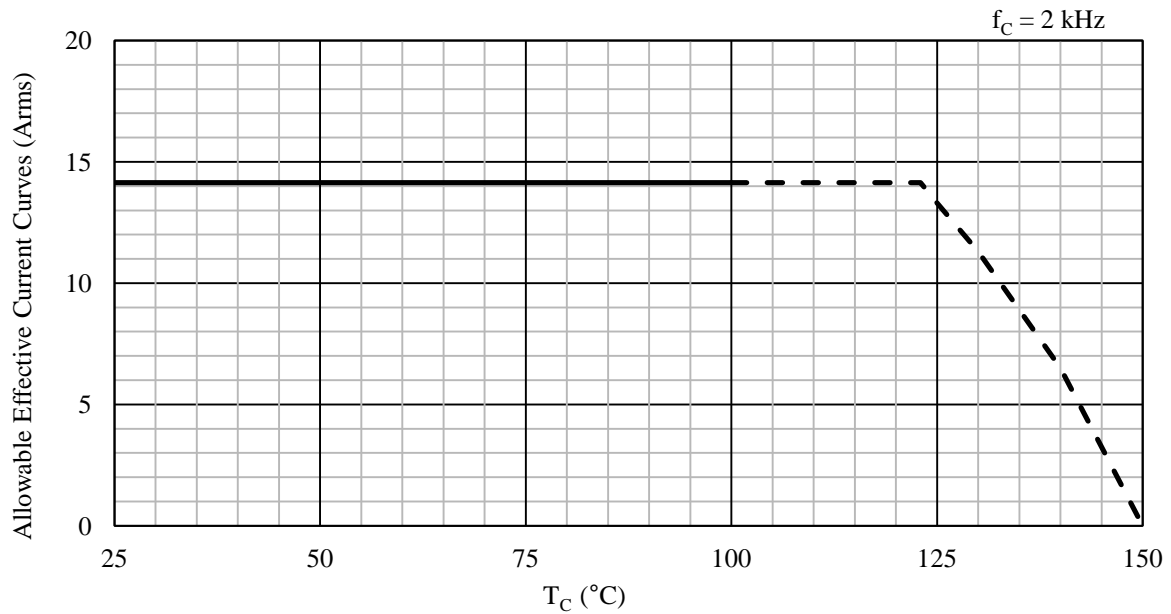


Figure 15-52. SCM1274MF Allowable Effective Current ($f_c = 2$ kHz)

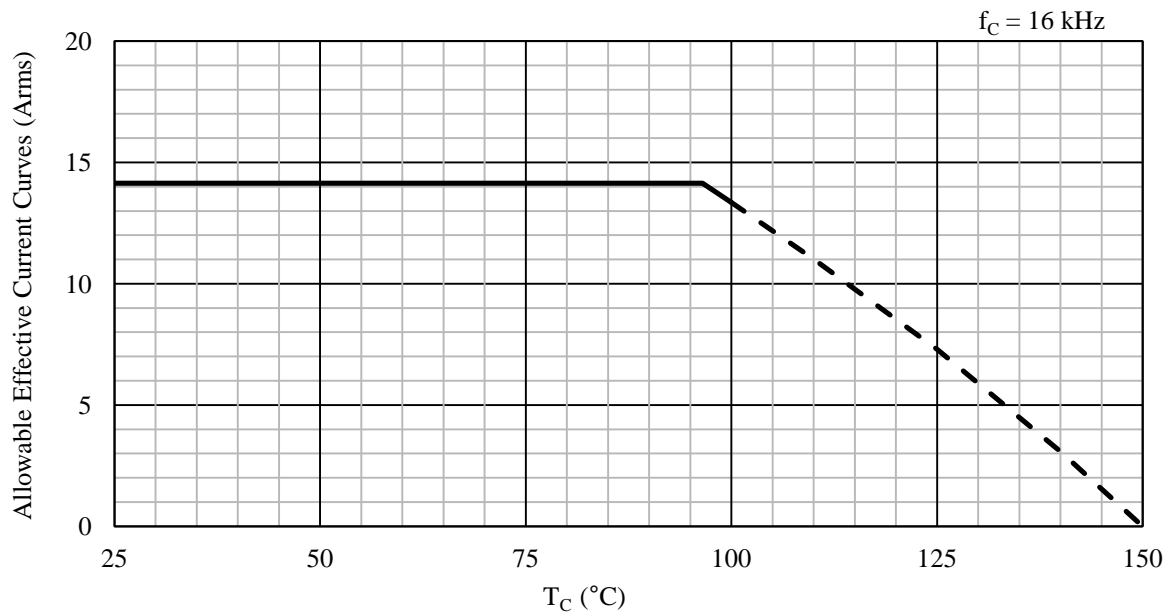


Figure 15-53. SCM1274MF Allowable Effective Current ($f_c = 16$ kHz)

15.4.4. SCM1276MF

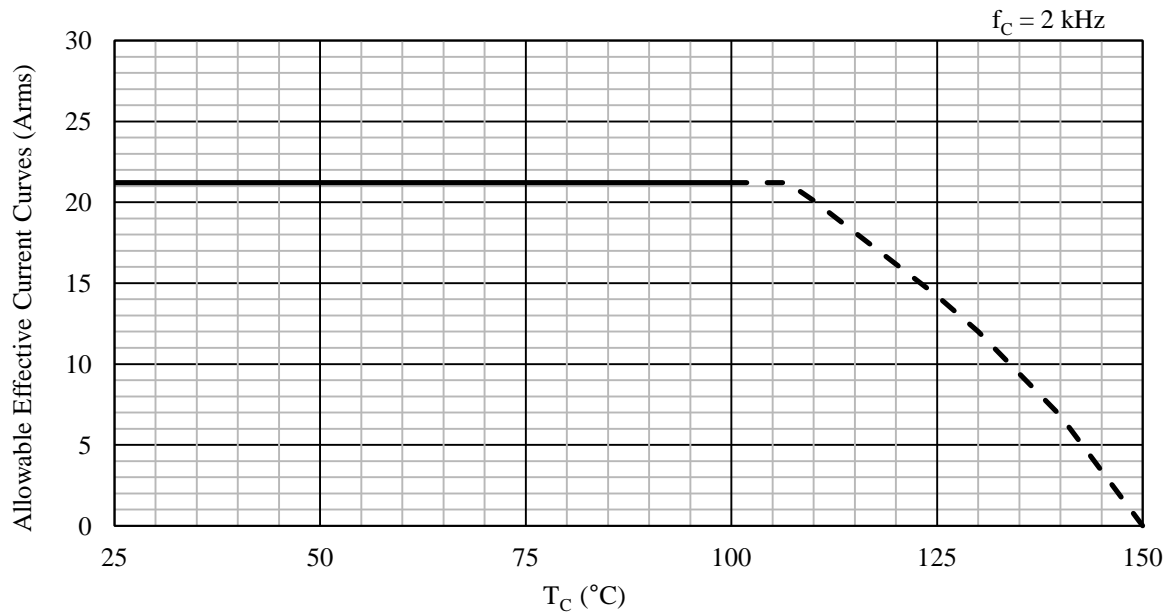


Figure 15-54. SCM1276MF Allowable Effective Current ($f_c = 2$ kHz)

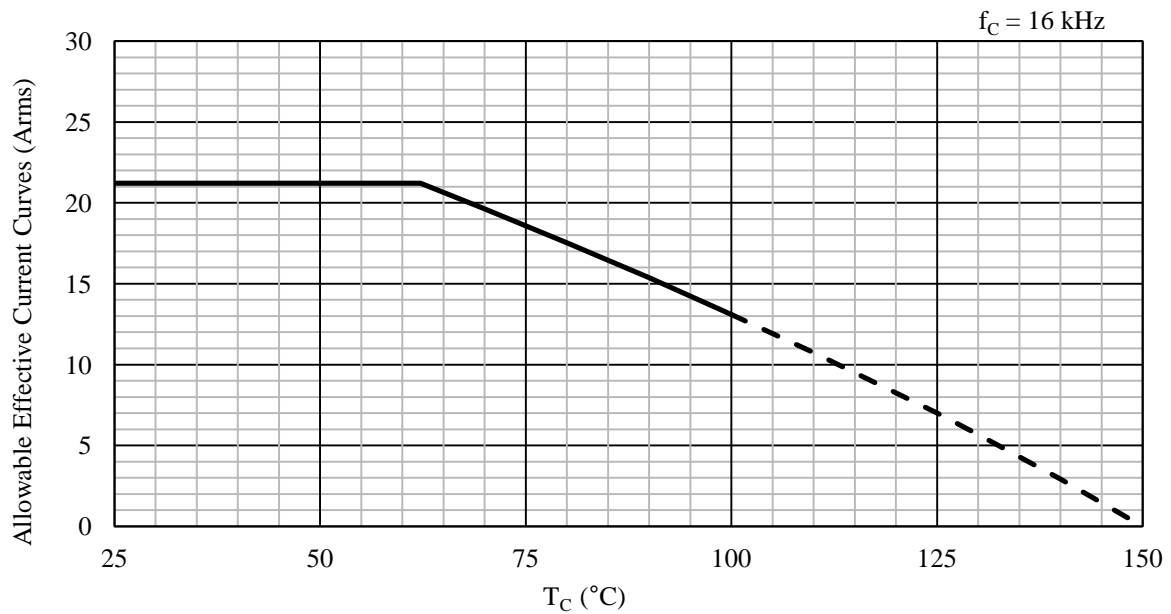


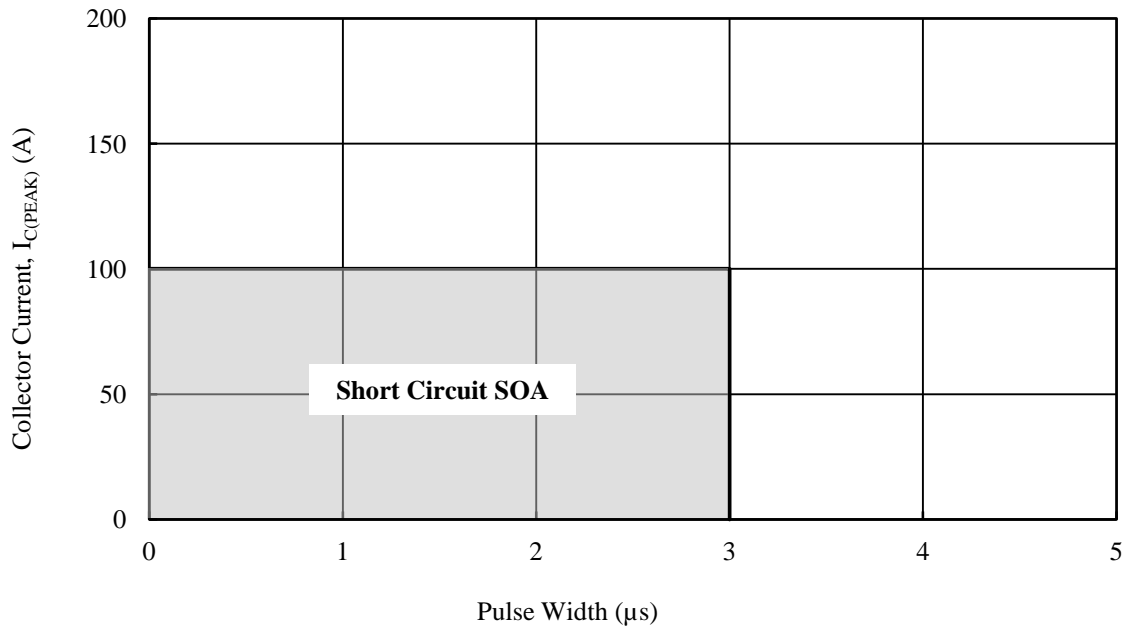
Figure 15-55. SCM1276MF Allowable Effective Current ($f_c = 16$ kHz)

SCM1270MF Series

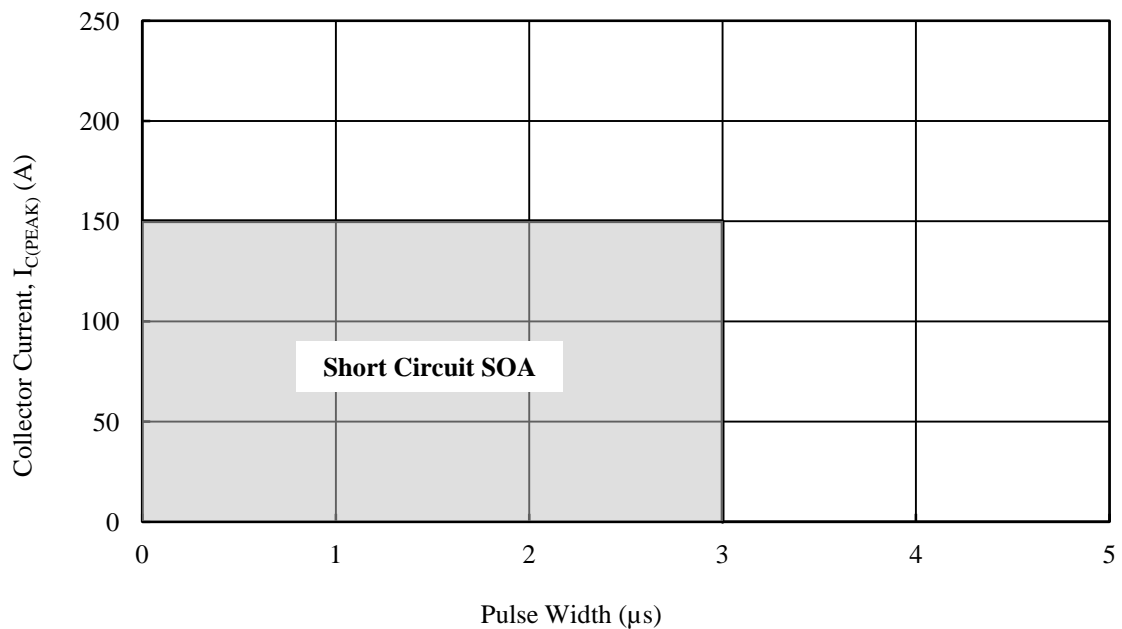
15.5. Short Circuit SOAs (Safe Operating Areas)

Conditions: $V_{DC} \leq 400 \text{ V}$, $13.5 \text{ V} \leq V_{CC} \leq 16.5 \text{ V}$, $T_j = 125^\circ\text{C}$, 1 pulse.

15.5.1. SCM1271MF

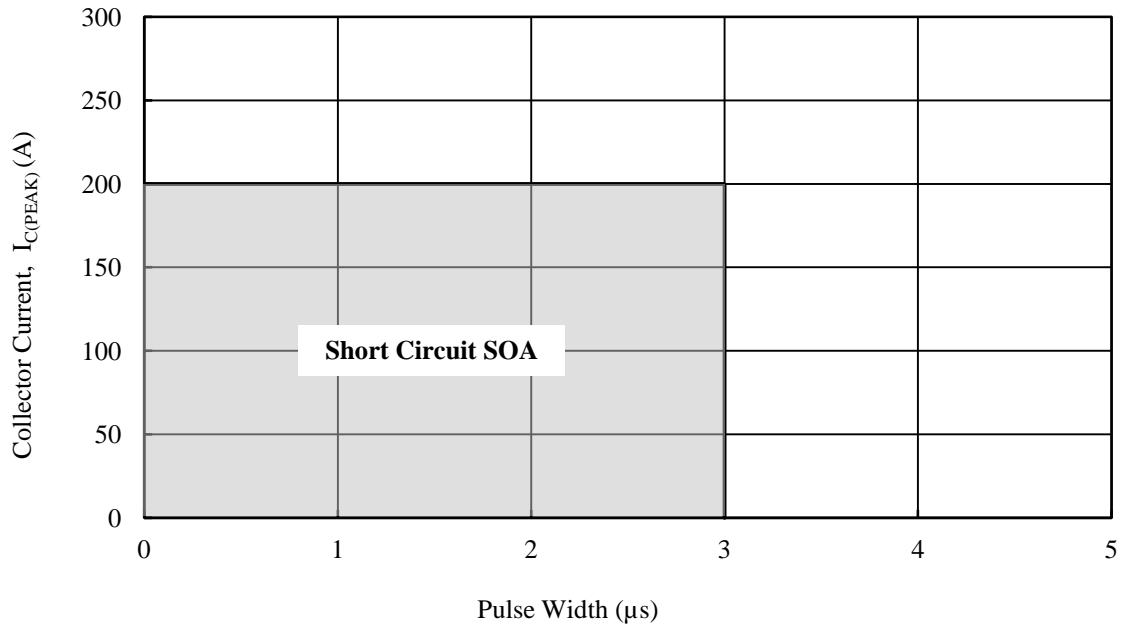


15.5.2. SCM1272MF

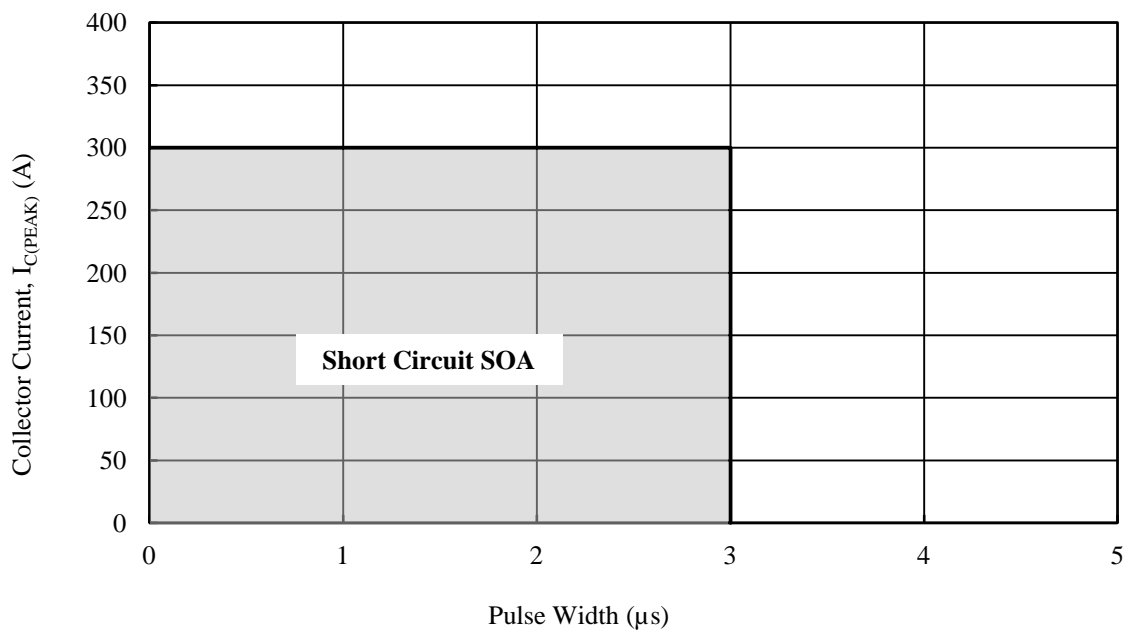


SCM1270MF Series

15.5.3. SCM1274MF



15.5.4. SCM1276MF



16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SCM1270MF series device. For reference terminal hole sizes, see Section 10.3.

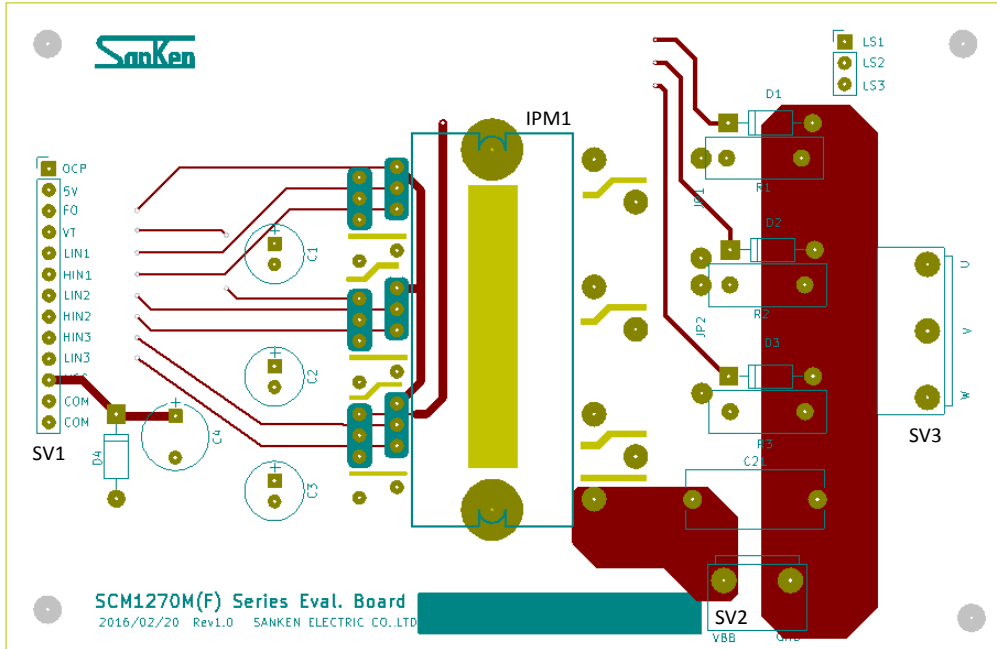


Figure 16-1. Top View

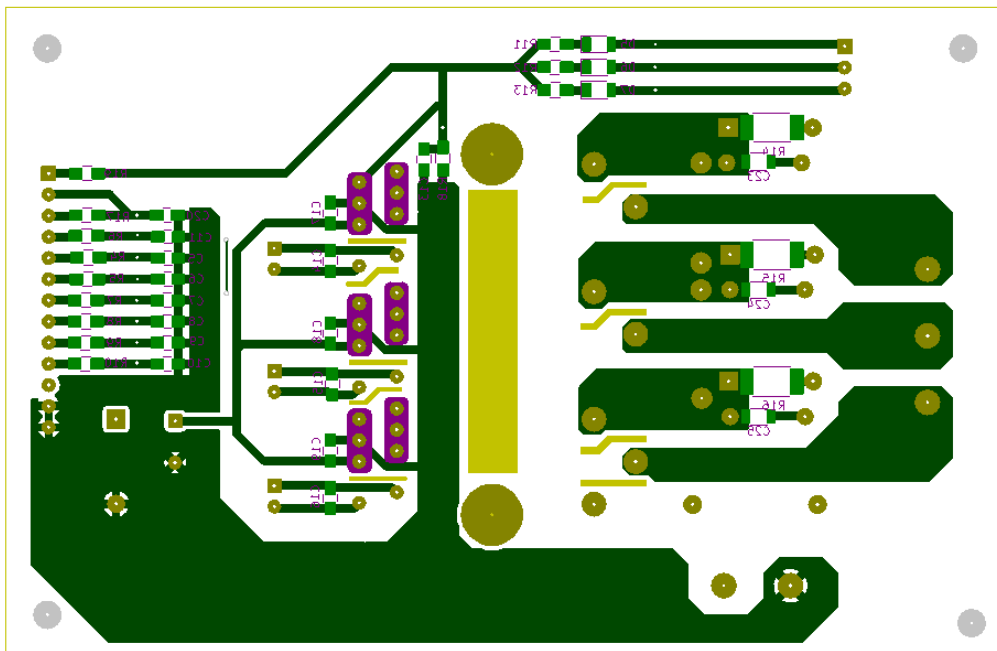


Figure 16-2. Bottom View

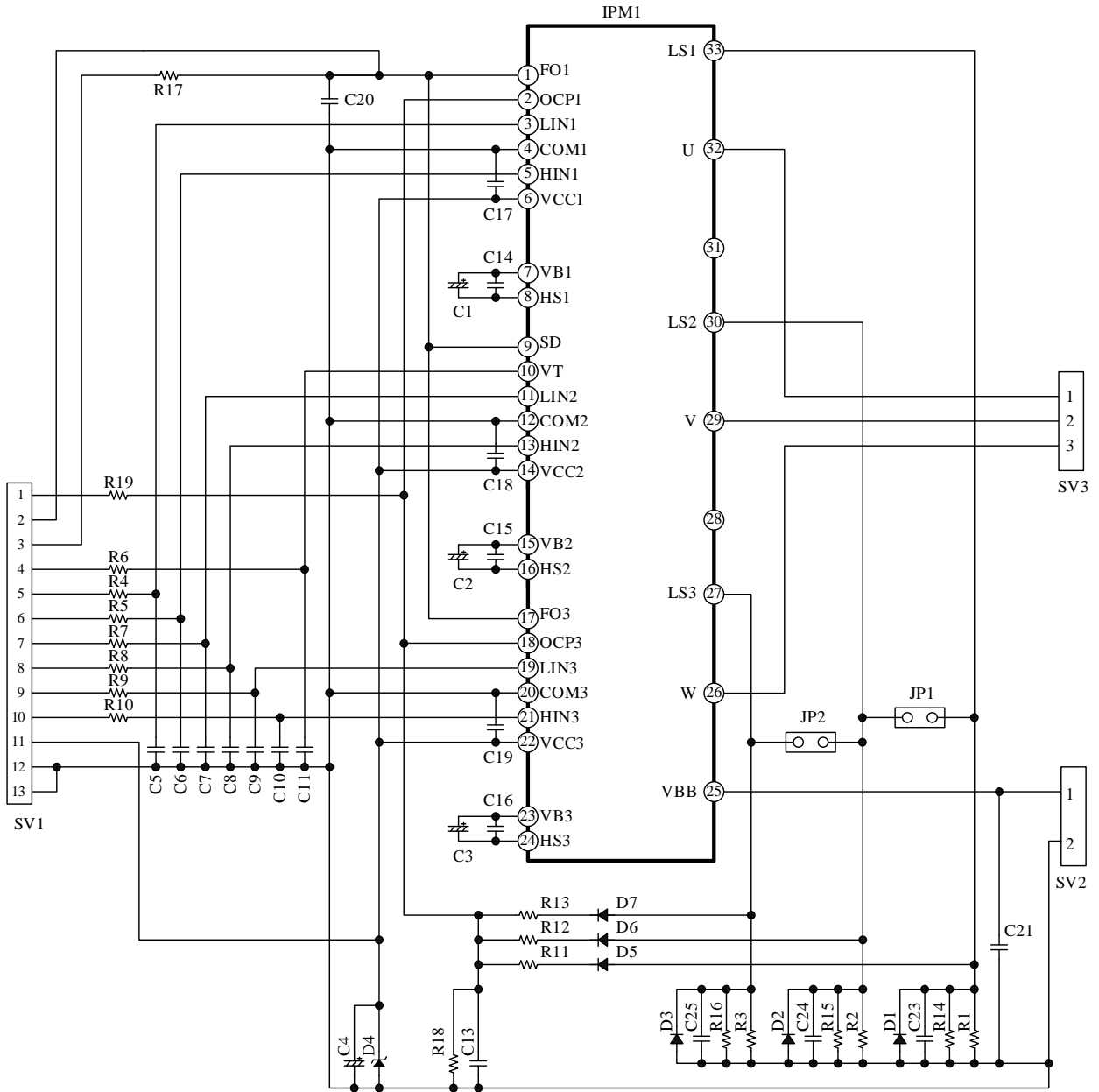


Figure16-3. Circuit Diagram of PCB Pattern Layout Example

SCM1270MF Series

17. Typical Motor Driver Application

This section contains information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SCM1272MF
Main Supply Voltage, V _{DC}	300 VDC (typ.)
Rated Output Power	1.35 kW

- **Circuit Diagram**

See Figure16-3.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	47 μF, 50 V	D5	General	1 A, 50 V
C2	Electrolytic	47 μF, 50 V	D6	General	1 A, 50 V
C3	Electrolytic	47 μF, 50 V	D7	General	1 A, 50 V
C4	Electrolytic	100 μF, 50 V	R1*	Metal plate	18 mΩ, 2 W
C5	Ceramic	100 pF, 50 V	R2*	Metal plate	18 mΩ, 2 W
C6	Ceramic	100 pF, 50 V	R3*	Metal plate	18 mΩ, 2 W
C7	Ceramic	100 pF, 50 V	R4	General	100 Ω, 1/8 W
C8	Ceramic	100 pF, 50 V	R5	General	100 Ω, 1/8 W
C9	Ceramic	100 pF, 50 V	R6	General	100 Ω, 1/8 W
C10	Ceramic	100 pF, 50 V	R7	General	100 Ω, 1/8 W
C11	Ceramic	100 pF, 50 V	R8	General	100 Ω, 1/8 W
C13	Ceramic	4700 pF, 50 V	R9	General	100 Ω, 1/8 W
C14	Ceramic	0.1 μF, 50 V	R10	General	100 Ω, 1/8 W
C15	Ceramic	0.1 μF, 50 V	R11	General	200 Ω, 1/8 W
C16	Ceramic	0.1 μF, 50 V	R12	General	200 Ω, 1/8 W
C17	Ceramic	0.1 μF, 50 V	R13	General	200 Ω, 1/8 W
C18	Ceramic	0.1 μF, 50 V	R14*	General	Open
C19	Ceramic	0.1 μF, 50 V	R15*	General	Open
C20	Ceramic	0.01 μF, 50 V	R16*	General	Open
C21	Film	0.22μF, 630 V	R17	General	3.3 kΩ, 1/8 W
C23*	Ceramic	0.1 μF, 50 V	R18	General	5.1 kΩ, 1/8 W
C24*	Ceramic	0.1 μF, 50 V	R19	General	100 Ω, 1/8 W
C25*	Ceramic	0.1 μF, 50 V	SV1	Pin header	2.54 mm pitch
D1	General	1 A, 50 V	SV2	Connector	Equiv. to B2P3-VH
D2	General	1 A, 50 V	SV3	Connector	Equiv. to B3P5-VH
D3	General	1 A, 50 V	IPM1	IC	SCM1272MF
D4	Zener	V _Z = 20 V, 0.5 W			

* Refers to a part that requires adjustment based on operation performance in an actual application.

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